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1

General Information

Product Overview

Features

Hewlett–Packard's J Class Workstations are based on a PA7200 central processing unit (CPU) that provides a variety of interfaces, graphics, and mass storage.

Table 1–1. J Class Features

Features	Functionality		
Operating system	HP–UX 9.05	HP–UX 10.0 must be used with multiprocessors	
CPU Performance			
	100 MHz	120MHz	120MHZ (J210XC)
PA–RISC PA7200			
MIPS:	196.3	237.2	
MFLOPS:	43.9	52.7	
SPECint92:	138.7	168.4	
SPECfp92:	221.4	266.0	
SPECrate_int92:		7790.9 (using 2 CPUs)	
SPECrate_fp92:		11745.5 (using 2 CPUs)	
External Cache			
Instruction cache size	256 KByte / 1 MByte/cpu (J210XC only)		
Organization	Direct mapped		
Bus width	64 bits		
Instruction cache bus peak performance	960MB/sec I–fetch (8 byte)		
Data cache size	256 KByte / 1 MByte/cpu (J210XC only)		
Organization	Direct mapped		
Bus width	64 bits		
Data cache bus peak performance	960MB/sec load (8 byte), 960 MB/sec single store (8 byte)		
Time source	Battery–backed Real–Time Clock		
Memory	16 slots 32 MB minimum required Upgradeable to 768 MB at HP–UX 9.05 Upgradeable to 1 GB at HP–UX 10.0		
Memory Management Unit			
Virtual memory address	48 bit		
Instruction TLB and data TLB	Unified 120 page entries, additional single–entry instruction TLB lookaside, 16 block entries, fully associative		

Table 1–1. J Class Features (Cont.)

Features	Functionality
Monitor Support	17–inch 1280x1024 color monitor or 20–inch 1280x1024 color monitor
Optional Graphics	2D color graphics (single and dual head) HCRX–8/HCRX–24 Fast 8–plane or 24–plane graphics HCRX–8Z/HCRX–24Z Accelerated 8–plane or 24–plane graphics CRX–48Z 24–plane Accelerated, double–buffered graphics Freedom series 3150 graphics subsystem w/1 MB texture memory Freedom series 3250 graphics subsystem w/1 MB texture memory Freedom series 3400 graphics subsystem w/1 MB texture memory
Graphics Performance Fast 2D Color HCRX–8, HCRX–24 HCRX–8Z, HCRX–24Z CRX–48Z	 Xmark93 11.7, GPC PLBwire93 83.6, GPC PLBsurf93 34.2 Xmark93 15.4, GPC PLBwire93 93.7, GPC PLBsurf93 43.1 Xmark93 15.4, GPC PLBwire93 94.7, GPC PLBsurf93 95.4 Xmark93 11.0, GPC PLBwire93 102.1, GPC PLBsurf93 138.5
Power supply – max input power – 664 Watts Max Continuous output power – 484 Watts	Five DC output voltages (+5V, +4.5V, +12V, +3.4V, and –12V) Also +15V auxiliary for standby.
Mass storage	Up to two of the following: 1GB, low profile, 3.5–inch, Fast, Wide Differential SCSI hard disk drive 2GB, low profile, 3.5–inch, Fast, Wide Differential SCSI hard disk drive Up to two (with no two alike) of the following SE SCSI devices: 5.25–inch CD–ROM SE SCSI disc drive 3.5–inch, 4–8 GB, 4–mm DDS–format SE SCSI tape drive 3.5–inch SE SCSI floppy disk drive
Network	Built–in ThickNet LAN AUI and TP (Twisted Pair) connectors for the 802.3 (ETHERNET) network. Connections to ThinLAN networks require an external transceiver.
I/O	Two 9–pin RS–232 ports One 25–pin HP parallel port 8–bit Single–Ended SCSI–2 interface 16–bit Fast, Wide SCSI–3 interface Keyboard port for PS2 mouse Keyboard port for HP HIL devices Audio and speaker output Microphone or audio input

Memory

Minimum memory is 32 MB of 60 ns 4 Mbit, or 128 Mbit of 60 ns 16 Mbit DRAMs, or a combination of both. 32 MB is the minimum required for the HP–UX operating system. Each workstation has 16 memory slots, labeled 0A, 0B through 7A, 7B.

Memory upgrades include:

HP A3026A 32 MB DRAM Upgrade, two 16 MB DRAM boards.
HP A3027A 128 MB DRAM Upgrade, two 64 MB DRAM boards.

Internal Storage Devices

The J Class workstation can have up to two fixed disk drives, and up to two (no two alike) removable media drives.

Fixed Disk Drives

HP A4117A 1.0 GB LP Fast, Wide 3.5–in disk drive
HP A4119A 2.0 GB LP Fast, Wide 3.5–in disk drive

Removable Media Drives

CD–ROM Drive

HP A4282A CD–ROM Drive

DDS Tape Drive

HP A4281A 4.0–8.0 GB, 4–mm DDS Tape Drive
HP92283A Box of five 60–meter DDS data cassettes
HP92283B Box of five 90–meter DDS data cassettes
HP92283K Package of two cleaning cassettes

Floppy Disk Drive

HP A4283A SCSI Floppy Drive
HP92192X High–Density Micro Flexible Disks (1.44MB Formatted Capacity) – box of ten diskettes

System Graphics

The supported monitors are:
A4032A 17–inch, 1280x1024 color monitor
A4033A 20–inch, 1280x1024 color monitor

The supported graphics boards are:
A4077A 2D color graphics
A4070A HCRX–8 accelerated 2D/3D wireframe, 8/8 bit planes w/8 overlay plane graphics
A4071A HCRX–24 accelerated 2D/3D wireframe, 24 bit planes w/8 overlay plane graphics
A4079A HCRX–8Z accelerated 3D solids, 8/8 bit planes w/8 overlay, PowerShade software
A4179A HCRX–24Z accelerated 3D solids, 24 bit planes, PowerShade software
A4074A CRX–48Z accelerated 2D/3D wireframe, 24/24 bit planes graphics, PowerShade software
A4078A Dual color graphics card
A4253A Freedom series 3150 graphics subsyustem with 1MB texture memory
A4254A Freedom series 3250 graphics subsyustem with 1MB texture memory
A4255A Freedom series 3400 graphics subsyustem with 1MB texture memory

Built–In Interfaces

System Unit Interfaces

The system board's built–in interfaces have ports on the workstation rear panel.

Audio Interfaces

The J Class workstations have audio input and output capability through external input and output connectors on the rear panel and through an internal speaker. The rear panel contains the Audio IN (Stereo line–in) and Mic (Mic–in), and Audio OUT (Stereo line–out) and Headphones (Headphone–out) connectors.

The audio connectors are standard stereo audio mini–jacks. Hewlett–Packard recommends using gold–plated plugs available through audio retailers for best quality recording and playback through the external connectors. The following is a summary of the workstation audio features:

- Audio Features — Programmable sample rates:
  8kHz, 16kHz, 32kHz, 48kHz, 11.025kHz, 22.05kHz, and 44.1kHz.

  Programmable output attenuation:
  0 to –96dB in –1.5dB steps

  Programmable input gain:
  0 to 22.5dB in 1.5dB steps.

  Input monitoring:
  16–bit linear, 8–bit u–law, or A–law coding
- Audio Inputs — Line–in

  Mono microphone compatible with 1.5V phantom supply
  (bias voltage supplied by the system)

  CD–ROM audio (if internal CD–ROM is installed)
- Audio Outputs — Line–out
  Headphone
  Built–in mono speaker
- Audio CODEC — Crystal CS4215

Table 1–2 summarizes the audio electrical specifications for this workstation.

Table 1–2. Audio Electrical Specifications

Frequency Response	25–20,000Hz
Input Sensitivity/Impedance	
Line in	2.0Vpk/47kohm
Microphone	22mVpk/1kohm
Max Output Level/Impedance	
Line Out	2.8Vpp/47kohm
Headphone	2.75Vpp/50ohm
Speaker (internal)	5.88Vpp/48ohm
Output Impedance	
Line Out	619ohm
Headphone	118ohm
Signal to Noise*	
Line Out	65dB
Headphone	61dB
Speaker	63dB
Line in	61dB
Microphone	57dB
THD (w nominal load)	
Line Out	–73dB
Headphone	–70dB
Speaker	–68dB
Line in	–75dB
Microphone	–73dB

* To convert from dB to number of significant bits use the formula:

$$n = \frac{dB}{20 \log_{10}} \approx \frac{dB}{6}.$$

For example, for 61dB S/N then n= 61/6 ≈ 10
significant bits, or in other words, about 6 bits of noise.

Keyboard Interfaces

The J Class workstation provides keyboard interfaces that allow either PS/2 or ITF keyboards. Consult the documentation that accompanies each input device for specific information concerning its use.

PS/2 Keyboard Interfaces

The PS/2 connectors provide an interface for the keyboard and mouse to the system.

ITF Keyboard Interface

The HP HIL connector provides an interface for the ITF Keyboard to the system and all HP HIL devices.

HP Parallel I/O Interface

The 25–pin HP Parallel I/O interface uses Centronics interface protocols to support peripheral devices such as printers and plotters. Consult the documentation that accompanies each peripheral device for specific information concerning its use.

Network Interface

The J Class has built–in ThickNet LAN AUI and TP (Twisted Pair) connectors for the 802.3 (ETHERNET) network. Connections to ThinLAN networks require an external transceiver. Your workstation will autoselect the correct network setting.

The IEEE 802.3 Ethernet Local Area Network (LAN) circuit provides both the AUI interface for conventional coaxial Ethernet and a direct interface to a twisted pair (TP) 10BASE–T network. Only one built–in interface can be used at a time. The system auto–selects the correct port that is being used. Ethernet is a 10 Mbit/s packet–switched serial interface employing Carrier Sense Multiple Access/Collision Detection (CSMA/CD). Table 1–3 lists the supported LAN adapters and other network devices.

Table 1–3. Supported AUI LAN Adapters and Devices

LAN Adaptor	Network Devices
HP 28641B ThinLAN Transceiver HP 30241A 10Base4 ThickLAN MAU	HP 28692A ThinLAN Hub Plus HP 28673A 10:10 LAN Bridge HP 28683A Fiber Optic Transceiver

RS–232 Serial I/O Interfaces

The RS–232 Serial I/O (SIO) ports on the J Class accept a variety of pointing devices or peripheral devices. Peripheral devices include printers, plotters, modems, and scanners. Consult the documentation that accompanies each peripheral device for specific information concerning its use.

The SIO ports are programmable, allowing the setting of such functions as bit rate, character length, parity, and stop bits. SIO Ports are used as interfaces for serial asynchronous devices to the CPU. The ports operate at up to a 19.2 K baud rate.

Table 1–4 shows the SIO connector pin listings. The serial connectors are 9–pin D–sub connectors. Signal names are those specified in the EIA RS–232 standard.

Table 1–4. Serial I/O Pins

Pin No.	Signal	Description
1	DCD	Data Carrier Detect
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Ground
6	DSR	Data Set Ready
7	RTS	Request To Send
8	CTS	Clear To Send
9	RI	Ring Indicator

Small Computer Systems Interface

Use the SCSI connectors to connect external SCSI devices such as DDS–format tape drives and CD–ROM drives. Consult the documentation that accompanies each SCSI device for specific information concerning its use. Refer to Appendix C of the *J Class Owner's Guide* for information about connecting SCSI devices to the workstation.

The primary function of the SCSI−2 interface circuit is to take data from the CPU bus, translate it to SCSI format, and transmit it down the SCSI bus to a mass storage device, and vice versa. A secondary function is to keep track of the status of the SCSI bus and inform the CPU of the status.

SCSI circuits must have terminating resistors installed on them. When using the external SCSI configuration, you must use an active SCSI terminator at the last external device on the SCSI bus. All other devices, external or internal, must not be terminated. Use only HP K2291 terminators to ensure reliable system operation.

Recommended SCSI−2 mass storage device bus addresses are listed in Table 1−5, and SCSI interface technical information is listed in Table 1−6.

Table 1−5. *Recommended SCSI−2 Bus Addresses*

Unit or Mass Storage Device	Recommended Bus Address
SCSI host controller	7
First Hard Disk Drive	6
Second Hard Disk Drive	5
DDS Tape Drive	3
CD ROM Disk Drive	2
SCSI Floppy	0

Note Arbitration priorities for the single–ended and fast, differential SCSI–2 buses follow the order 7 through 0. Never use SCSI address7 for any device. Address 7 is always reserved for the host SCSI controller.

Table 1−6. *SCSI−2 Interface Technical Information*

Function	Data
Type:	SCSI–II (ANSI X3.131–1986), single–ended
Data rate:	Synchronous – 5 MBs/second
Device limits:	7 internal and/or external peripherals
Connector type:	SCSI–II, ALT–1 50–pin high–density thumb-screw
Maximum external cable length:	4 meters (13.1 feet)

Single–Ended SCSI–2

The built–in SCSI–2 port is implemented using an NCR710 macrocell inside the I/O ASIC chip. This 8–bit single–ended implementation is synchronous and compatible with the current 700 series products and supports 5 MB/sec data transfer rates.

The SCSI bus is terminated to 3.3 volts through 127kΩ on the CPU board. If an external disk drive is used, an active terminator must be used on the drive at the end of the cable.

Fast, Wide Differential SCSI–3

Fast, wide SCSI is an extension to the existing 8–bit, single–ended SCSI. “Fast differential” indicates that signals on the SCSI bus are differentially driven and terminated , and capable of a 10 MHz clock rate. “Wide” indicates that there are 16 data bits on the SCSI bus.

The fast, wide SCSI bus is specified at a peak synchronous transfer rate of 20 MB/sec. The architecture of the fast, wide SCSI port on the J Class workstation has been designed to allow a 20 MB/sec sustained transfer rate for long data streams.

Power Cord Connector

Plug the workstation’s power cord into the power cord connector to provide ac power to the system.

Hardware Architecture

The J Class is a mid–tower style designed to be easy to operate and upgrade. The features in this package are designed for user access to the majority of the system's upgradable parts (disks, memory SIMMs, and processors) without moving the system.

Figure 1–1 shows the front view of the system. There is a Power Switch with an LED to indicate that the system is on/off, and an LCD panel that informs users of the system's status. In the case of a failure, the LCD indicates the failure code.

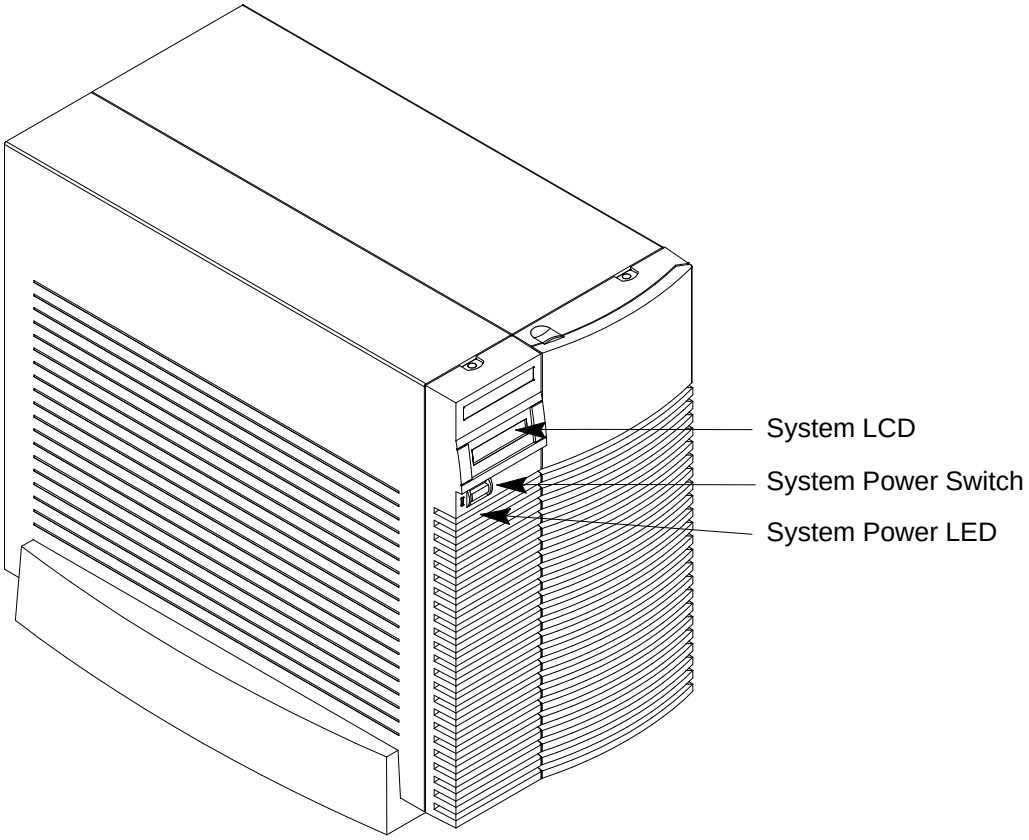

Figure 1–1. System Unit Front Panel Controls

Figure 1–2 shows a peripheral door for removable media(s). This door can be removed (snap) and re–installed easily.

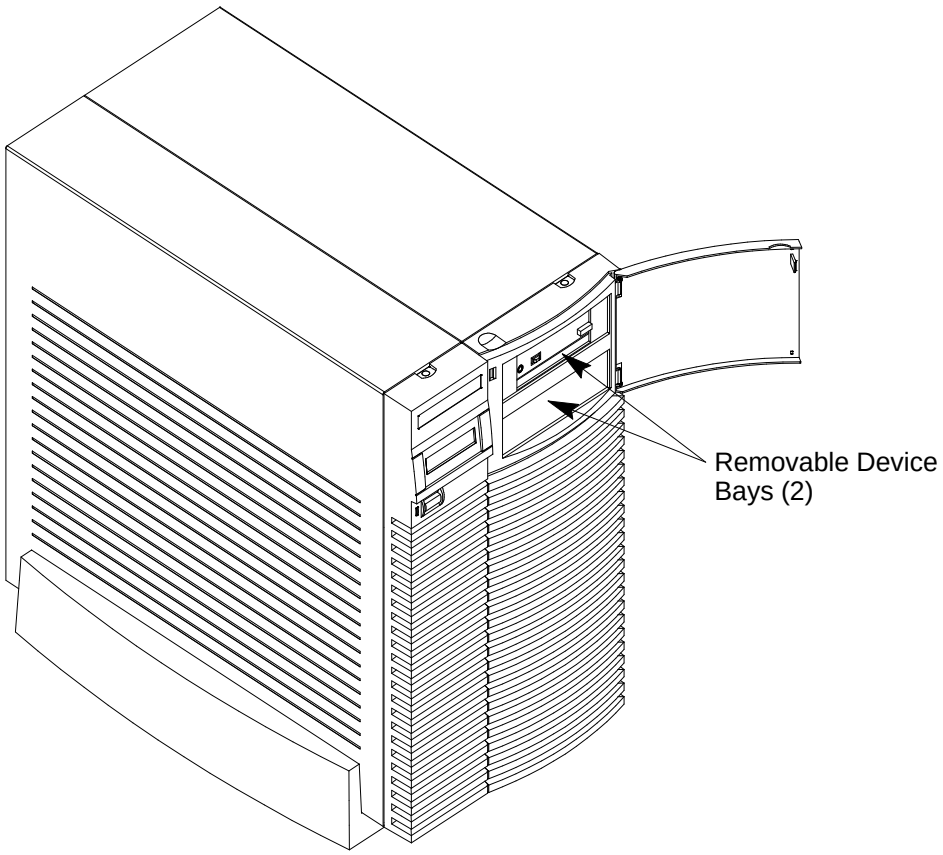

Figure 1–2. System Unit with Removable Device Door Open

The front bezel can be detached by pushing down on two snapping locks located on top of the bezel and chassis. By removing this front bezel, you can access the system board, power supply, and peripheral bay. All these Field Replaceable Units (FRU's) can be detached easily and removed for upgrade or repair.

There are two more FRU's that are accessed from the back of the system: the I/O card and EISA cardcage. There are two external SCSI connectors available for external devices to be used with this product.

Operating System

HP–UX

HP–UX 9.05 and 10.0 are supported on the Model J200 and J210 workstations. HP–UX is booted from an internal hard disk drive factory installed with Instant Ignition. HP–UX can also be installed from external DDS or CD–ROM drives. If the workstation is a client on LAN, HP–UX can be booted over the LAN. Table 1–7 lists the HP–UX operating systems and languages for the workstation.

HP–UX 10.01 is support on the Model J210XC only.***more info about 10.01 needed?***

Table 1–7. HP–UX Operating Systems and Languages

Operating Systems	HP–UX 9.05, 10.0, or 10.01 HP–UX 9.05 complies with the UNIX® System V Interface Definition, X/Open, and POSIX Specifications and will be fully compliant with Operating Systems Foundation (OSF) HP–UX 10.0 complies with IEEE POSIX 1993.1 and 1003.1 FIPS 151–2 ANS X3.159–1989, System V Interface Definition (SVID) Issue III (Base System and all Extensions, with exceptions), X/Open Portability Guide Issue IV (XPG4) (Base Branding), and OSF/Motif 1.2. HP–UX 10.0 also complies with IS 9945/1 and Base Component and all Optional Components except XTI only. HP–UX 10.01 (Model J210XC only)***more info needed?***
X Window System	Version 11 Release 5 (X11R5), OSF/Motif 1.2
Languages	C/ANSI C, C++ FORTRAN 9000 Pascal PA–RISC 1.1 Assembler COBOL
User Interface and Graphics Libraries	HP VUE 3.0 X11R5, PEX, PHIGS Starbase capabilities HP PowerShade

Product Identification

A label on the back of the J Class workstation lists the product's serial number. For example, serial number 6247A00001 is interpreted as follows:

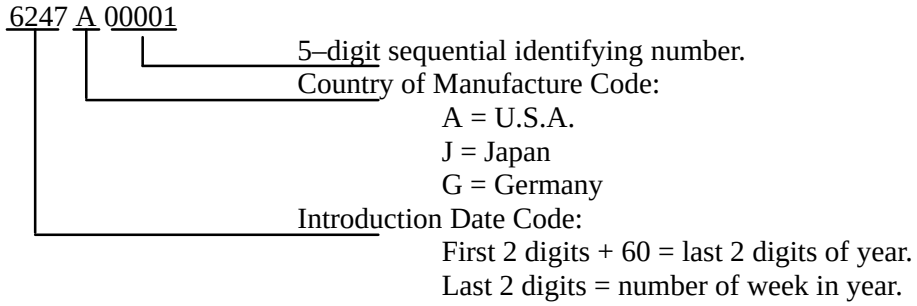
6247 A 00001
5–digit sequential identifying number.
Country of Manufacture Code:
A = U.S.A.
J = Japan
G = Germany
Introduction Date Code:
First 2 digits + 60 = last 2 digits of year.
Last 2 digits = number of week in year.

Figure 1–3. Product Serial Number Label Interpretation

Board Exchange Part Numbers

HP A2375–69057 CPU Module, 100MHz (Model J200)
HP A2375–69056 CPU Module, 120MHz (Model J210)
HP A****–**** CPU Module, 120MHz (Model J210XC)
HP A4081–69001 System PCA
HP A4081–69002 EISA Backplane PCA
HP A4072–69512 HCRX Z–Accelerator Board
HP A4073–69001 GSC interface for use with CRX–48Z
HP A4070–69504 HCRX–8
HP A4071–69507 HCRX–24
HP A4081–69009 Color Graphics Card

Board Nonexchange Part Numbers

HP A4081–60004 I/O Connector PCA
HP A4081–66011 Jumper PCA
HP A4081–66007 SCSI Disk PCA

Support Documentation

Table 1–8 and Table 1–9 list the service and support documentation.

Table 1–8. Service Documentation

Manual Title	Part Number
Service Handbook; J Class Workstation	A4081–90602
Service Handbook Update	A4081–90605
HP A4032/A4033 Color Monitors CE Handbook	A4033–90099

Table 1–9. System Installation and Getting Started Documentation

Manual Title	Part Number
J Class Hardware Installation Guide	A4081–90601
J Class Owner's Guide	A4081–90600
Notice Regarding J Class Processor	A4277–90600
Installing Additional Memory	A4081–90606
SCSI Tech Data	5951–7100
HP–UX Device Driver Manual	98577–90014
SCSI Tech Reference Manual	98265–90010
HP–UX 9.05 Manuals	
Using your HP workstation	A2615–90001
HP Vue User's Guide	B1171–90061
HP Vue Quick Start Guide	B1171–90080
HP–UX 9.05 Series 700 Release Notes	B2352–90611
Read Me First HP–UX 9.05	B2352–90614
HP–UX 9.05 PCO Read Me	A4081–90604
Installing HP–UX	B2355–90039
Installing Peripherals	B2355–90041
HP–UX 10.0 Manuals	
Using your HP Workstation	A2615–90003
HP Vue 3.0 User's Guide	B1171–90079
HP Vue Quick Start Guide	B1171–90080
HP–UX 10.0 Release Notes	B3782–90011
Read Me First HP–UX 10.0 s700	B3782–90033
Installing HP–UX 10.0	B2355–90050
Configuring HP–UX for Peripherals 10.0	B2355–90053
HP–UX 10.01 Manuals	
**	

Regulatory and Safety Information

Regulatory Compliance

- Federal Communications Com. (FCC)
  47 CFR Part 15
  Subpart J, Class B
  VCCI Class 1
- Industry Canada for Class B

Product Safety

- Underwriters Laboratories (UL) listed UL 1950
- Canadian Standards Assoc. (CSA) certified CSA 22.2 950M
- TUV, license to EN60950
- EMKO TUE(74) DK203

Electromagnetic Compatibility (EMC) Directive

- EN55022/CISPR 22 Class B
- EN55024–2/IEC801–2
- EN55024–3/IEC801–3
- EN55024–4/IEC801–4

Ergonomics

- TUV ZH1/618
- ISO9241
- 90/270 EEC

System Processing Unit

- Physical Dimensions (See Figure 1–4
- Weight

Min. configuration	80 lbs (36 kg)
Fully loaded	92 lbs (42 kg)

- Power Source Consumption

  11.5 Amps RMS max @ 100 Vac, 50 Hz
  5.3 Amps RMS max @ 220 Vac, 50 Hz

Auto ranging	90 – 132 Vac or 198 – 264 Vac
Line frequency	47 – 63 Hz
Max. power input	664 watts

- Environmental Specifications

Altitude	Operating	0 − 15,000 ft
	Non−operating	0 − 40,000 ft
Magnetic field interference		
	Operating	< 5 Gauss (ac peak−to−peak or dc) at 4 product surfaces
	Non−operating	< 5.25 milligauss dc at 15 ft.
Electromagnetic Interference (EMI)		
	Emissions	FCC Class B
	Susceptibility	FCC Class B
Electrostatic Discharge		
	Air discharge	0−15 kV, no effect
	Contact discharge	0−3 kV, no effect
Humidity (Non−condensing)		Operating 15 to 80%
Leakage Current		less than 3.5 mA
Shock		
	Operating	20 g at less than 3 ms, 1/2 sine in normal axis with no hard errors
	Non−operating	80 g at less than 3 ms, 1/2 sine
Temperature		
	Operating	+5 − 40 degrees C
	Non−operating	−40 − +70 degrees C
Vibration		
	Operating random	0.21 G rms, 5 − 500 Hz
Swept sine survival		0.5 G peak, 5 − 500 Hz
Random survival		2.09 G rms, 5 − 500 Hz

Reliability

Estimated Annualized Failure Rate (AFR) is based on a parts count and the failure rates of those parts in similar products. The AFR is estimated from the sum of the failure rates of the components' assemblies. A key assumption is that AFR is constant beyond the early life of the product and before long–term wear out. Mean Time Between Failures (MTBF) is the reciprocal of the AFR. Table 1–10 shows the AFR and MTBF of the J Class, with and without mass storage.

Table 1–10. AFR and MTBF

Product	Configuration	AFR	MTBF
J Class	32 MB, no mass storage	22.0%	39,818
J Class	32 MB, with mass storage	25.5%	34,350

Projected Failure Rate is the mature AFR, estimated from the failure rates of the components of the product. The "Estimated Long–Term Annualized Failure Rate" is a future projection of an average realistic failure rate beyond the typical infant failure period that occurs in the first few months of use and before long–term wear out which occurs after many years of use. These rates are for a full year and are based on a 100% duty cycle.

Mechanical Specifications

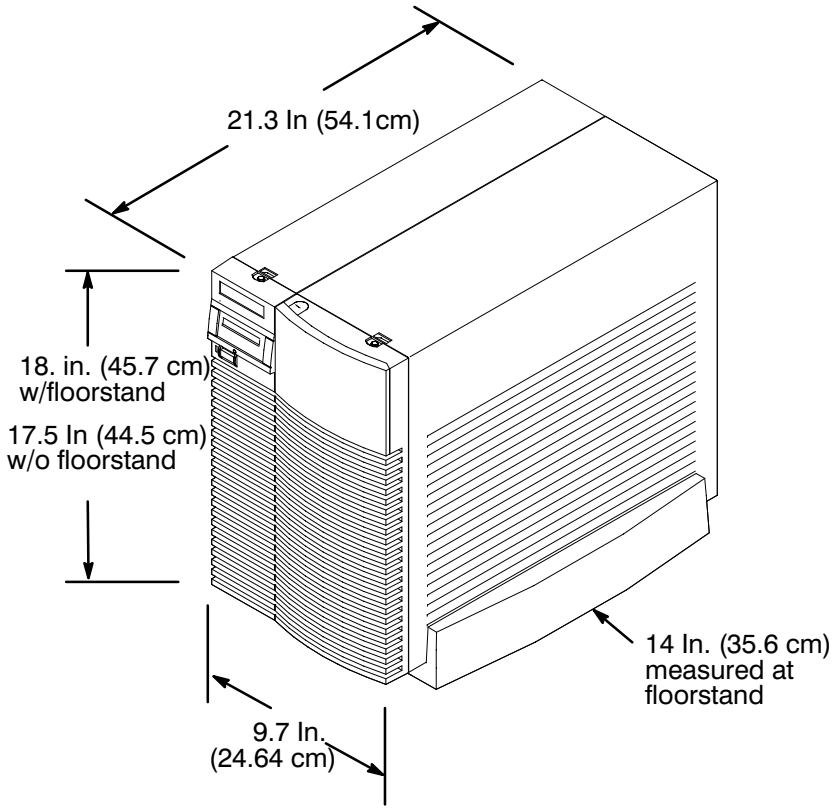

Figure 1–4. Chassis Dimensions

System Board Assembly

This board contains several daughter cards, the CPU modules (2), the Memory SIMMs (16), and the ON/OFF system status. It can be accessed and replaced from the system front. There is also a daughter board that has the LCD for system status. The following is a detailed specification of this board:

Part Number:	A4081–66001
Size:	approx. 14” x 15”
Weight:	less than 15 lbs
# of Layers:	12
# of Connectors:	16 + 16 memory slots

Back Plane

This board interconnects I/O, the power supply, the system board and the peripheral assembly. It is mounted to the chassis and requires some mechanical tools to disassemble. The following is a detailed specification of this board:

Part Number:	A4081–66003
Size:	approx: 10” x 8”
Weight:	less than 10 lbs
# of Layers:	6
# of Connectors:	12

Peripheral Assembly

This assembly can be easily removed from the front of the chassis. It contains two removal drives and two hard drives. It has two external connectors (FW,SE) for external–to–chassis connections. It connects to the back plane through a daughter card in the bay. The following is a detailed specification of this section:

NOTICE: Removal of the peripheral assembly is for ease of maintenance and upgrading. It is NOT for data security.

Part Number:	A4081–62002
SCSI Interface Card Part Number:	A4081–66007
Size:	16” x 6” x 4”
Weight:	less than 8 lbs
Size of the Daughter Card:	9” x 5”
# of Layers for Daughter Card:	6
# of Connectors:	6

GSC/EISA Assembly

This section contains a sheet metal bay enabling users to install up to five I/O slots (4 EISA boards and up to 3 GSC+ boards). It connects directly to the system board through a connector and has an EISA/GSC back plane. The following is a detailed specification of this cage:

Part Number:	A4081–62007
EISA B/P Part Number:	A4081–66002
Size:	7.5” x 6.7” x 5”
Weight:	less than 10 lbs
EISA B/P PCB Size:	7.5”x 6.7”
EISA B/P PCB # Layer:	6
# of Connectors:	10

I/O Assembly

The I/O board connects directly to the system back plane and contains all of the system's external I/O connections (See Figure 1–4 in *HP9000 J Class Owner's Guide*). This board is removed from the back of the system. The following is a detailed specification of this board:

Part Number:	A4081–66004
Size:	9" x 5"
Weight:	less than 4 lbs
# of Layers:	4
# of Connectors:	7

Power Supply

This section contains the power supply PCB and two 80 mm fans. It directly connects to the system back plane via blind mate connectors and delivers 484 watts of power to the rest of the system. This subsystem can be removed from the front of the chassis without disconnecting any cables except the AC Line Cord from the back of the system chassis.

Part Number:	0950–2497
Size:	434mm X 317mm X 90mm
Weight:	6 Kg
# of Connectors:	3 Output Connectors / 1 Input Connector
Type of Connectors:	Output Connectors are Molex "Minifit" Blind Mate Input Connector is IEC320 compatible

Power System Specification

The J Class Power Supply is 484 watts at 75% efficiency which delivers all the proper voltages to the system. It contains two 80 mm fans designed to deliver the proper airflow to all sections in the system. Power is distributed through "blind mate" interconnects to the system backplane, minimizing the number of internal power cables and easing manufacturing and field servicing of the system. The power system budget is shown in Chapter 7 of this document. There are two voltage regulators on the system board. One converts +5v to +2v and the second converts –12v to –3.2v. These two regulators provide power to the clock circuits. There is also a voltage regulator on the EISA backplane which converts –12v to –5v for EISA power. The system is turned On/Off via the front panel switch.

LCD Display Board

The control panel module is a 16–character x 2–line display. The display is connected to the System board by a single 14–pin connector located directly in back of the Hitachi Module Board. Note that the J Class implementation requires a special viewing angle part. The "industry standard" part is a 6:00 view as implemented in a calculator. That optimizes a viewing angle looking from the bottom. The J Class part optimizes a 12:00 viewing angle from the top.

Mechanical Data :

Hitachi Part Number	LMO71L
Size	80w x 36h x 11t max mm
Viewing Angle Direction	12:00 +– 20 deg
Effective Display Area	64.5w x 13.8h mm
Character Size (5x7)dots	2.95w x 3.8h mm
Character Pitch	3.65h mm
Weight	approx 25 g

Electrical Data :

Power For Logic	VDD – Vss 0 min 6.5v max
Power For LCD	VDD – Vo 0 min 5.0v max
Power Supply Current	(VDD = 5.0v) 1.0ma typ 3.0 ma max

Air Flow

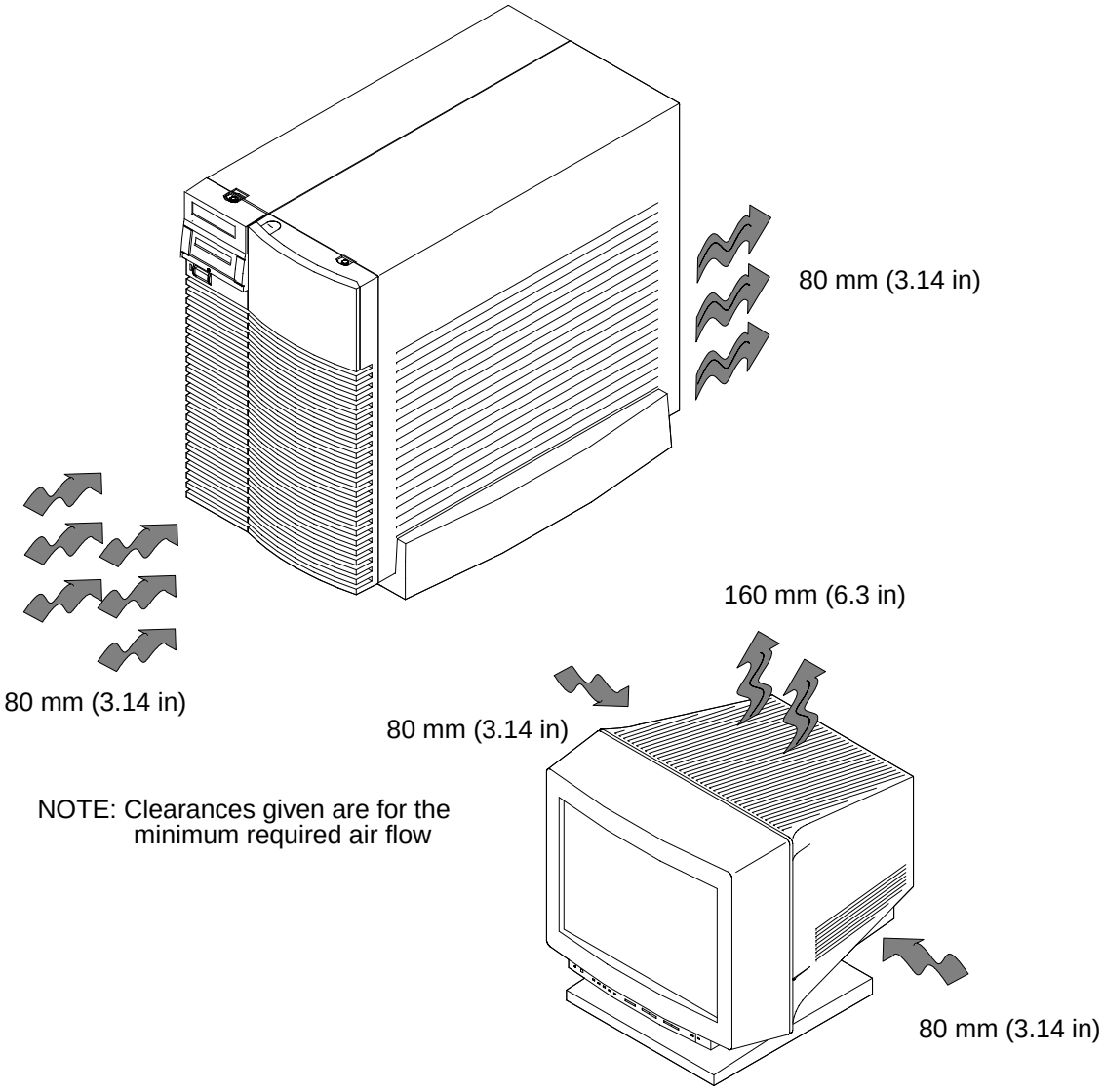

Figure 1–5. J Class Air Flow

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2

System Overview

Chapter 2 contains the following system information:

- Functional information on the system board, including a system unit block diagram
- Specifications for the system board interfaces
- Descriptions of the 2 CPUs
- A description of the CPU–Memory–I/O Interconnect

Functional Information

The system board contains:

- Two processor modules
- 16 Memory SIMMs

This board can be accessed and replaced from front of the system. There is also a daughter board that has the power ON/OFF and LCD for system status. The following is the detailed specification of this board:

FRUs	**PART NUMBER**
System Board	A4081–66012
Processor Module	A2375–66056 (Model J200 – 100 MHz)
Processor Module	A2375–66057 (Model J210 – 120 MHz)
Processor Module	A2375–60008 (Model J210XC – 120 MHz)
16 MB SIMM	A2579–60001
64 MB SIMM	A2580–60001

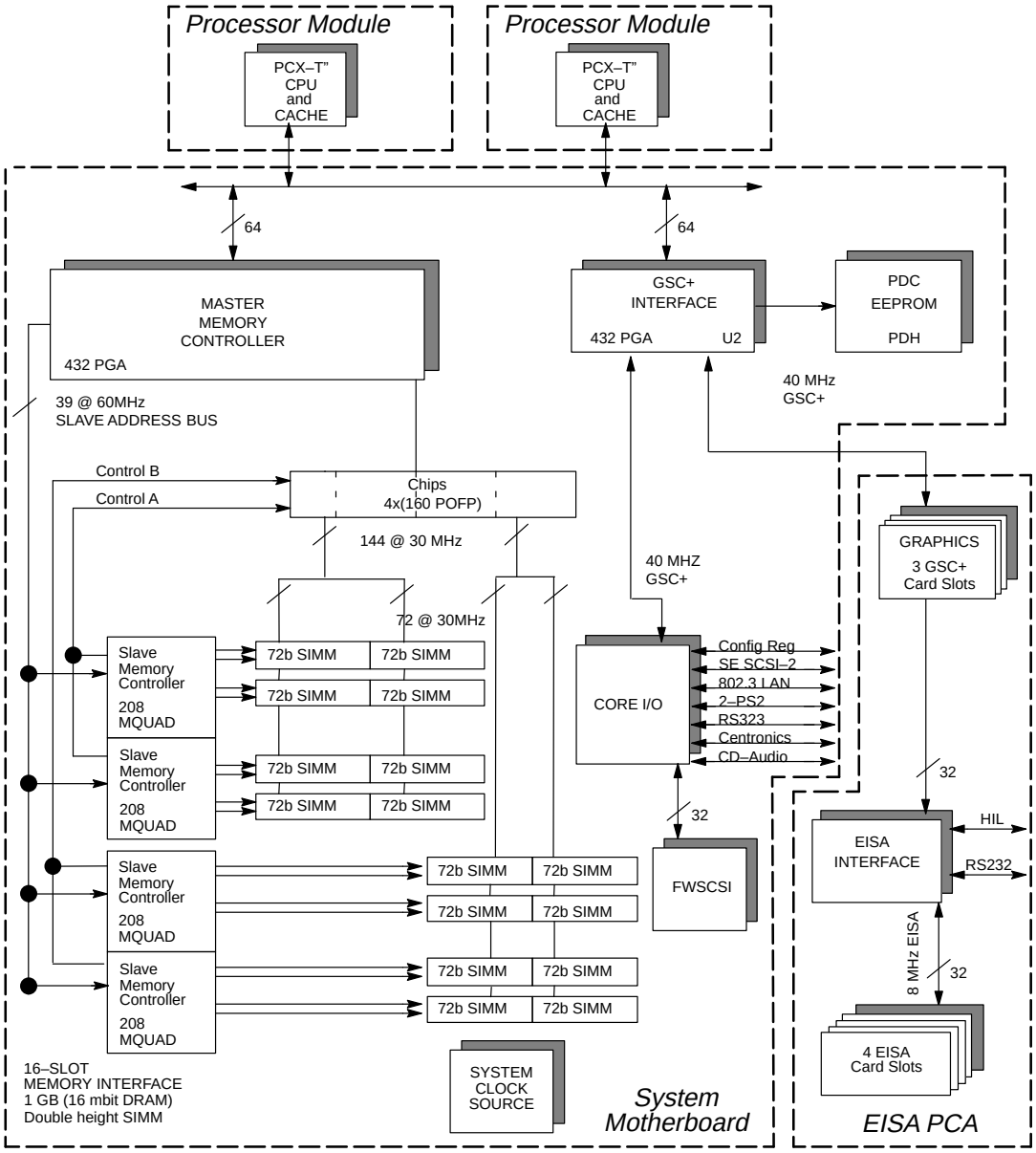

Figure 2–1. System Unit Functional Block Diagram

Interface Specifications

This section contains specifications for the LAN interface, the RS–232C port, the HP Parallel port, and the PS/2 interfaces.

Below is a summary of the LAN interface on the system board:

- Intel 82596CA LAN Controller functionality.
- IEEE 802.3/Ethernet 1.0.
- Boot ROM source support for diskless.

Table 2–1 lists the LAN interface technical information.

Table 2–1. LAN Interface Technical Information

Function	Data
Type:	IEEE 802.3, Ethernet 1.0
Data rate:	10 Mbits/second
Connector types:	AUI LAN – 15–pin Twisted Pair – 8–pin

RS–232C

The RS–232C port is full modem control with RTS hardware flow control. The port is implemented using a 9–pin male D–sub connector. Some devices that are supported on RS–232C include modems, plotters, printers, terminals, digitizers, and other input devices.

Table 2–2 lists technical information for the RS–232C interface.

Table 2–2. RS–232C Technical Information

Function	Data
Type:	RS–232C
Baud rate:	19.2 K
Word size:	5 to 8 bits
Parity, number of stop bits	Odd, even, one, zero, none
Device Type:	1 per interface connector
Connector Type:	9–pin male D–sub connector

HP Parallel

The Parallel Interface is an 8–bit parallel, synchronous interface commonly used for printers. The hardware implementation has bidirectional capabilities compatible with PS/2 standards, also know as Centronics R interface. The hardware is also capable of interfacing to BiTronics type printers that transmit status information back to the workstation. Table 2–3 lists technical information for the HP Parallel interface.

Table 2–3. HP Parallel Interface Information

Function	Data
Type:	Centronics, NACK and BUSY handshakes
Data rate:	>400 Kbytes/second with DMA 250 Kbytes/second sustained
Device Limit:	1
Connector Type:	25–pin female DB25 connector

PS/2

The keyboard and mouse interfaces are implemented by simple serial ports conforming to the defacto industry standard PS/2 specification. Both the keyboard and mouse have a dedicated serial port of their own. The interface ports rely on the software to provide all of their intelligence; therefore, they do not interpret the characters passing through them in either direction. The interface to the host processor is through 6 one–byte registers for each port. The keyboard and mouse are connected to the system via standard PC–style, miniature DIN connectors. The keyboard is a PC compatible 101 and 102 key layout PS/2–style with a cable length of 7.5 feet. The 3–button mouse (A2839A) comes with a 9 foot cable. The mouse can be ordered separately. We do not recommend extending the keyboard or mouse cables beyond 15 feet, due to signal degradation.

Central Processing Units

This section describes the J Class CPUs, processor module, and cache memory.

CPU

General Overview

The PA7200 CPU module is designed to work with J Class workstations. It offers the next step in performance after the 7150 PCX–T based module. Not only does it offer a higher performance processor, the bus interface also provides higher bandwidth than its predecessor. Finally, the bus and processor support symmetric multi–processing, and hardware based cache coherency. The CPU module consists of a processor, split Instruction and Data cache, and a bus interface. Different performance points can be achieved by adjusting three factors: processor clock frequency, bus clock frequency, and cache size.

Introduction

The electrical interface between the CPU module and the rest of the system is composed of power, clocks, the interconnect bus interface, and test interface. Most power and ground and all logical signals are routed through an impedance controlled Micropax connector. The two remaining power sources, VDH and VDL are routed through 2 Metral power connectors. Identification of the module clock rate, cache size, and processor voltage requirements are provided with static lines, hardwired on the module.

Signal Description

Micropax and Metral Power Connectors

The CPU module has 2 Metral power connectors and a single 200–pin Berg Micropax connector as its external system interface.

The 2 Metral power connectors receive Vdh and Vdl from the external system. Each Metral power connector consists of two receptacles. In the J Class systems, only one power receptacle is used at any one time. The Metral connectors also serve as alignment pins to guide the CPU module onto the system board.

Vdd and all logical connections are connected through the 200–pin Micropax connector. The signal pad pitch is 25 mils and the pads are placed in 2 rows in an offset pattern. There are 124 logical signal pins, 16 Vdd pins, 57 Ground pins, and 2 +12 volt and 1 no connect (spare). The signal to ground ratio is 2:1.

Please refer to Table 2–4 for a summary of the interface signals and power bus. Also, refer to the Micropax Connector Pinout.

Table 2–4. CPU Interface Signal and Power Bus Summary

Group	Signal Type	Pin Quantity	Comment
Bus Interface	Uni, Bi− directional	94	Some are unused
Test	JTAG	5	
Module Configurations Status	Uni − Static	8	
Clocks	ECL	12	
Pow_On		1	
Reserved		1	
Ground	Power	57	
VDD	Power	16	
+12 V	Power	2	
VDH	Power	1	Metral connector. Only one pin used,
VDL	Power	1	Metral connector. Only one pin used,

Bus Interface

Table 2–5 specifies the interconnect bus signals, bussed on and off the CPU module.

Table 2–5. Interconnect Bus Interface Signal List

Signal	Signal Count	Direction *	Comments
ADDR_DATA[0:63]	64	Bi−dir	**
ADDR_PAR[0:1]	2	Bi−dir	**
ADDR_VALID	1	Bi−dir	**
ARB_IN[0:2]	3	Input	
ARB_OUT	1	Output	
CLIENT_ID[0:3]	4	Static Input	Tied on system board.
CLIENT_OP[0:2]	3	Input	
COH[0:1]	2	Output	Point−to−Point
CTL_PAR	1	Bi−dir	**
DATA_VALID	1	Bi−dir	**
LONG_TRANS	1	Bi−dir	**
IOA_ARB_IN[0:1]	2	Input	
MASTER_ID[0:2]	3	Bi−dir	**
TRANS_ID[0:2]	3	Not_used	Tied low on module.
TRANS_ID[3:5]	3	Bi−dir	**

* With respect to CPU
** Arbitrated for as a group; winner drives all these signals.

Test Access Port (TAP)

The CPU module supports the IEEE 1149 standard. Please refer to Table 2–6 for a summary of the Test Access Port signals. These signals are routed to the modules system interface to assist in manufacturing testability.

Table 2–6. Test Access Port (TAP) Signal Summary

Signal	Signal Count	Direction	Comments
TCK	1	Input	Test clock
TMS	1	Input	Test Mode Select
TDI	1	Input	Test Data In
TDO	1	Output	Test Data Out
TRESET	1	Input	Reset Tap

Module Configuration Status

The CPU module is able to identify its cache size, operating frequency, and processor operating voltage requirements. The clock frequency status ensures that a module is not installed in a system with a system clock frequency that is incompatible with the module. Please refer to Tables 2.11, 2.12, 2.13, and 2.14 for a further description of the configuration status byte.

Table 2–7. Module Configuration Status Byte

Status [0:7]							
0	1	2	3	4	5	6	7
Cache Configuration			**Operating Frequency**			**Operating Voltage**	

Status[0:5] are supplied to the Processor Dependent Hardware (PDH). PDH is able to detect the presence or absence of a CPU module in a slot by reading the first two status bits of the module. Each of the bits is pulled high through a resistor on the system board. The CPU module ties the bits that should be logic zero to ground through a 0 ohm resistor.

Table 2–8. Cache Configuration Bits

Status[0:2]			Cache Size − Bytes	
0	1	2	I Cache	D Cache
0	0	0	64K	64K
0	0	1	256K	256K
0	1	0	1M	1M
0	1	1	Reserved−J200 and J210	Reserved−J200 and J210
0	1	1	512K−J210XC	512K−J210XC
1	0	x	Reserved	Reserved
1	1	x	No CPU present	

Table 2–9. Operating Frequency Configuration Bits for J200 and J210

Status[3:5]			Clock Frequency
3	4	5	
0	0	0	Reserved
0	0	1	100MHz
0	1	0	120MHz
0	1	1	Reserved
1	x	x	Reserved

Table 2–10. Operating Frequency Configuration Bits for J210XC

Status[3:5]			Clock Frequency
3	4	5	
0	0	0	160MHz (PCX−U)
0	0	1	100MHz
0	1	0	120MHz
0	1	1	180MHz (PCX−U)
1	0	0	200MHz (PCX−U)
1	0	1	240MHz (PCX−U)
1	1	0	Load Board
1	1	1	No CPU Present

Status[6:7] are routed directly to the power system, which senses the configuration before supplying power to the system. Each of the bits is pulled high through a resistor in the power supply. The CPU module ties the bits which should be zero to ground through a 0 ohm resistor.

Table 2–11. Operating Voltage Configuration Bits

Status[6:7]		Nominal Processor Operating Voltage
6	7	
0	0	5.0 Volts
0	1	4.4 Volts
1	0	Reserved−J200 and J210
1	0	3.3 Volts−J210XC (PCX−U)
1	1	Power supply, ignore cpu slot, processor not present.

Processor Module

Overview

The PA7200 Processor Module family is a modular concept for processor board design. The PA7200 Module family encompasses two clock frequencies to provide various price/performance points for

different system applications.The Central Processing Unit for the PA7200 Module family is the PA7200 CPU chip, which is an evolution of the high–performance single chip superscalar PA7100 CPU design. The PA7200 implements the 3rd edition of the PA–RISC 1.1 Architecture, documented in the *PA–RISC 1.1 Architecture and Instruction Set Reference Manual*. This latest design implements a number of design improvements that increase system performance for both technical and commercial applications including increased frequency, instruction and data cache prefetching, enhanced superscalar execution, and enhanced multiprocessor support. The PA7200 connects directly to a new split transaction, 768 Megabytes/second multiprocessor memory and I/O bus. This enables high performance multiprocessor systems without requiring additional processor interface components, further improving the price/performance of a PA7200 based system. The PA7200 CPU chip is fabricated in HP's proprietary CMOS14 technology which features 0.55 micron devices with three levels of metal interconnect packaged in a 540–pin PGA.

Features

The PA7200 supports the following features:

Feature	Description
Clock Frequency	120 MHz Maximum
Superscalar	Integer/integer and integer/floating point superscalar execution
Multiprocessor	Cache coherency support
Hardware static branch prediction	

FP Features

Feature	Description
Coprocessor	On–chip 64–bit internal data paths
Fully pipelined ALU and MPY units	Fully concurrent ALU and MPY operation

External Cache Features

Feature	Description
Instruction/data cache	256K (each)
64–bit access	Direct–mapped
Hashed address	Virtual index
Parity error detection on I/D caches, correction on I–cache	
32–byte cache line size, copy–back STORE policy	

Internal Cache Features

Feature	Description
Fully associative on–chip data cache	64 cache lines
FIFO queue	Accessed in parallel with external cache
3 data prefetch modes	
1. No prefetch	
2. Only on modify–after–miss	
3. Any miss or first access	
1 miss and up to 4 prefetches in parallel	
No allocate cache hint	
Instruction prefetch buffer	1 cache line

TLB Features

Feature	Description
MMU	120–entry unified I/D TLB
Fully associative	NRU replacement
4K–page size TLB	1–entry ITLB lookaside buffer
16–entry, 512K–64M BATC	Hardware TLB miss handler support
Level–1 PA implementation (48–bit virtual address)	Up to 4–GBytes physical memory

Interface Features

Feature	Description
System interface	processor–memory–I/O interconnect bus:
Split transactions	768–MByte/sec
Coherent I/O support	120 MHz max. frequency
Supports 1:1 and 3:2 CPU	processor–memory–I/O interconnect bus clock frequency ratios
Test/diagnostics support	IEEE 1149.1 interface
DIAGNOSE instructions	Single–step and N–step

Cache Memory

General Overview

Cache Organization

The J200 and J210 processor Instruction cache size is 256K bytes. The J210XC processor –Instruction cache size is 4K bytes to 1M bytes . The constraining factor in implementing a particular cache size is the availability of SRAM with the correct timing specifications. The key difference between this processor's cache implementations and that of other HP workstation models, is that the write pulse width has been shortened to one clock cycle from two. This requirement is necessary due to copy–ins from the interconnect bus that deliver a double word, compared with Previous Generation Processor bus (Pbus) that transferred one word at a time.

I–Cache

The I–Cache is a single set associative cache or direct–mapped cache. For the J200 and J210 CPU module, the instruction cache size is 256KB. For the J210XC CPU module, the instruction cache size is 1Mbyte . The cache for the J200 and J210 is organized as 32K deep by 64 bits. The cache for the J210XC is organized as 128K deep by 64 bits . The 64 bits constitute a double word instruction fetch providing the capability of performing dual instructions for clock cycle. To perform instructions simultaneously, the instructions must be a certain combination. Prior to writing the double word out to cache, the CPU determines if the instructions can be bundled. If so, the predecoded information is written out to the cache along with the double word.

The double word in the I–Cache is protected by word parity. In the case of an I–cache parity error, the line is marked invalid and the CPU must fetch the line from memory. Reads and writes are all done on a double word basis.

D–Cache

The D–Cache is also a single set associative or direct–mapped cache. Similar to the I–Cache, the J200 and J210 CPU module has a data cache size of 256KB. The J210XC CPU module has a data cache size of 1Mbyte. The cache for the J200 and J210 is organized as 32K deep by two 32–bit single words; the data tags are addressed separately. The cache for the J210XC is orgainized as 128K deep by two 32–bit single words; the data tags are addressed separately. The D–Cache tags have their own address bus (TADH), and tag bus (DCTH) in order that the tag may be read earlier than the data. The D–Cache also has a double word read, but for writes each word can be written independently. Separate writes for each word allow the word to be written without performing the read and modify.

Each word in the D–Cache is parity protected. There is no ECC on the D–Cache. Thus, if there were a single bit error on a dirty line, the machine must HPMC. If the line is clean then, like in the I–Cache, the line can be marked invalid and fetched from memory.

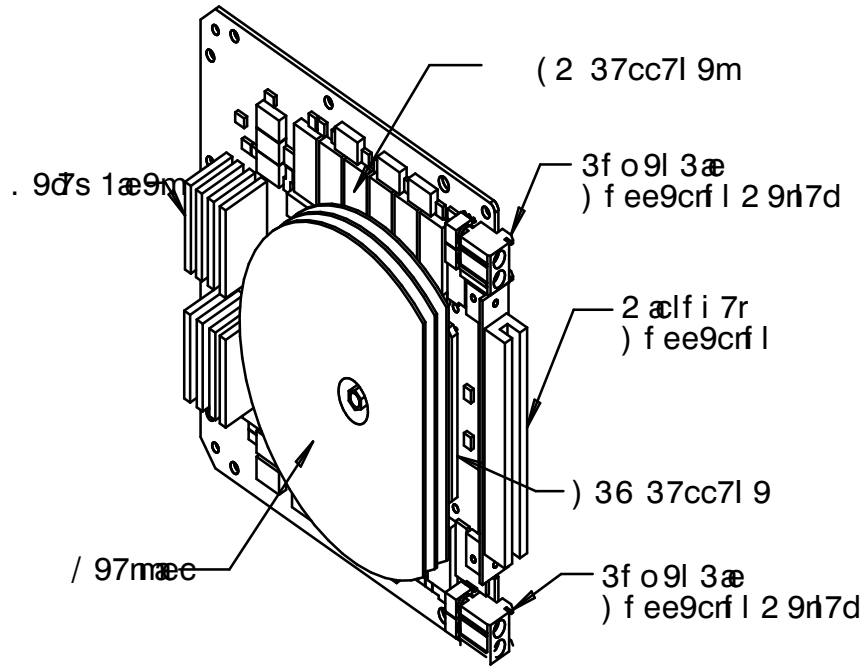

Figure 2–2. CPU Module

CPU–Memory–I/O Interconnect

Introduction

J Class workstations support one or two processors and a single U2 I/O adapter (containing two IOAs) on a single interconnect bus that implements a snoopy coherency protocol. This section summarizes the major points of the processor–memory–I/O interconnect bus.

Features

The interconnect bus has the following features:

- Provides a price/performance competitive bus for 1–4 way (maximum of 2–way on J Class) multiprocessing, for high–end workstations and mid–range servers
- Provides leadership–effective memory latency
- Minimizes interface complexity
- Spans both technical and commercial markets
- Supports cache coherent I/O
- Performs multiple outstanding transactions per module, up to 64
- Protocol supports maximum frequency for shared bus
- Multiple coherency checks in process simultaneously

- Supports coherent I/O, with special transactions for DMA in either 16–byte blocks or cacheline–sized blocks.
- No aborts or retries
- No dead cycles for master turn–around
- Single cycle transaction issue; no separate SADD/MADD/VADD cycles
- 40–bit physical address support.

Overview

Peak bandwidth depends on frequency and linesize. Each memory transaction, either read or write, is made up of a single address cycle, plus 2, 4, or 8 data cycles, for 16, 32, or 64 byte lines respectively. Thus, as the linesize increases, more of the signal bandwidth is used for data transfer, so larger linesizes deliver a greater effective bandwidth.

To achieve maximum frequency, the protocol is designed so that no logic needs to be done in the same cycle as a chip crossing, and there are no OR–tied signals.

Multiplexes Address / Data Bus

The bus is a 64–bit wide time–multiplexed address/data bus. On each data cycle, a full doubleword of data is transmitted. On each address cycle, all information needed to issue the transaction is transmitted, including transaction type, address, and cache index.

ID−Tagged Split Transactions

All split transactions are tagged with the issuing module's MASTER_ID and a transaction ID, such that the combination of MASTER_ID, transaction ID, and return–type are unique for the duration of the transaction. The data response is identified by the same MASTER_ID and transaction ID, so that an extra address cycle is not needed for the data return.

Decoupled Coherency Reporting

Each module can report cache coherency (CCC) status on coherent transactions at its own rate, rather than at a fixed time. Each module has a dedicated bus to report CCC status, in FIFO order, to the central host. As long as each coherent module has reported CCC status by the time the data is ready to be returned, there is no extra delay for CCC.

No Abort Flow Control

The bus does not have any "retry" or "abort" signals or transactions. Instead, it uses predictive flow control, so that a transaction can only be issued if it can be handled. Previous busses have used a reactive flow control that aborted transactions after they were issued when some module signaled that it couldn't handle the transaction.

Other Features

Here are the other high points of the bus protocol:

- Single cycle address transfers
- No dead cycles between master changes
- 40–bit physical addressing
- 10–bit virtual index
- Maximum of 8 clients per bus, with clients being a mix of processors and other devices

- Split transactions
- Up to 64 outstanding transactions per client supported
- 32–byte cache line supported (restricted by memory and IO design)
- Snoopy coherency protocol
- Coherent I/O supported
- Address/Data and Control parity protection
- Supports EISA as a Lower I/O Bus

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3

Memory System

General Overview

Major features of the design are:

- High–performance design (low latency, high bandwidth)
- 36–bit Real Addresses (32GB)
- Supports 4Mbit, 16Mbit and 64Mbit DRAM Technology
- Supports 4GB of Memory with 64Mbit DRAMs, 1GB of memory with 16Mbit DRAMs
- Minimum memory increment of 32MB (4Mbit DRAM technology, x4 DRAMs, 2 banks of memory on 2 SIMMs)
- Coherent I/O
- Multi–Client support via snoop coherency and Interconnect Bus
- 32 Byte cache lines
- Memory Interleaving: 4–way per slave, maximum of 16–way interleaving
- Single bit error correct, double bit error detect, single DRAM failure detected for x4 and x8 parts Address included in ECC encode/decode to aid in hardware characterization and debugging
- Memory test and initialization for 2 GB of memory in less than 5 minutes
- Hardware Memory Scrubbing is **not** implemented
- 16 and 32 byte direct write access to memory. For smaller size writes, clients must read a line, modify it, and write it back
- IEEE 1149.1 boundary scan in all VLSI parts

The memory system uses multiple, independently controlled, sequentially interleaved, banks of Fast Page Mode DRAM memory to produce up to 768 MB per second (960 MB per second with EDO DRAM) of maximum data throughput. Multiple memory banks cycle at a rate of 12 MHz (15 MHz for EDO) per 32 bytes of data, on 2 independent DRAM Data buses.

The J Class memory system uses conventional, asynchronous, DRAM technology in the memory design because of its volume availability, low cost, and large capacity characteristics. The memory system design supports FPM (Fast Page Mode) DRAM, as well as having the potential for greater performance through the use of EDO (Extended Data Out) DRAM when supplier uncertainty can be resolved. SDRAM technology was not considered an alternative due to the uncertainty surrounding its definition and availability at design time.

Most of the operation references in this section are for the Fast Page Mode design. The EDO configuration is capable of higher bank throughput than the Fast Page Mode. The EDO bank cycles in 4 clocks (at 60 MHz), while the FPM bank cycles in 5 clocks. Future EDO enhancements are possible, especially in the 16 Mbit and 64 Mbit generations, depending on DRAM availability.

Memory System Block Diagram

The J Class memory system is constructed from four major components: the Master Memory Controller, Slave Memory Controllers, plug in memory modules (SIMMs), and data accumulate/MUX chips (DRAM Data Path MUX). Figure 3–1 shows a block diagram of the J Class memory system.

The basic unit of memory is called a *bank*. Each bank of memory is 16 data bytes wide and can be accessed independently from all other banks. A 32–byte cache line is read or written in two chunks using page mode accesses to a bank; two pieces of data are transferred to/from a bank to make up a cache line.

Each multibank DRAM controller chip supports up to four independent memory banks. Since system performance is highly dependent on the number of banks, the SIMMs are designed so that each SIMM contains eight data bytes of two banks. Since a bank is 16 data bytes wide, the minimum memory increment is two SIMMs, which yields two complete banks. The two banks on the two SIMMs have independent address and control signals. 16 bits of ECC are included for each 16 bytes (128 bits) of data, so a memory data bus carrying 16 bytes of data requires 144 bits total (128 data + 16 ECC = 144 total).

The 16–byte data bus (MD_H) that connects the Master Memory Controller chip to the DRAM Data Path MUX chips operates at 60MHz, for a peak bandwidth of 960MB/sec. Memory banks are connected to the DRAM Data Path MUX chips via 16–byte data buses (RDA_H, RDB_H). The RDA and RDB buses can deliver two 16–byte pieces of data every four, five, or six 60MHz cycles, depending on whether the transaction is a EDO read, a non–EDO read, or a write, respectively. These correspond to peak RDx_H bandwidths of 480MB/s, 384MB/s, or 320MB/s, respectively. However, the RDx_H buses are independent, so if memory accesses map to alternate buses, the peak bandwidth available from RDA_H and RDB_H equals the peak bandwidth of MD_H. The actual bandwidth depends on the memory access pattern, which in turn depends on the workload, the processors, and other factors.

The set of signals connecting the Master Memory Controller chip to multibank DRAM Controller and DRAM Data Path MUX chips is collectively known as the MSI bus (Master Slave Interconnect).

A single cache line transfer requires two cycles of data on MD_H and RDx_H. Since data is transferred over RDx_H at 1/2 the speed of MD_H, the DRAM Data Path MUX chips are responsible for accumulating and distributing data between the MUX data bus (MD_H) and the RAM data buses (RDx_H). Also note that to reduce the cost of the DRAM Data Path MUX chips, the design is bit sliced across 4 identical chips. In other words, each DRAM Data Path MUX *chip set* consists of 4 identical DRAM Data Path MUX chips.

J Class systems use one set of DRAM Data Path MUX chips as shown in the block diagram, and four multibank DRAM controller chips. This allows for up to 1GB of memory (16Mb DRAMs).

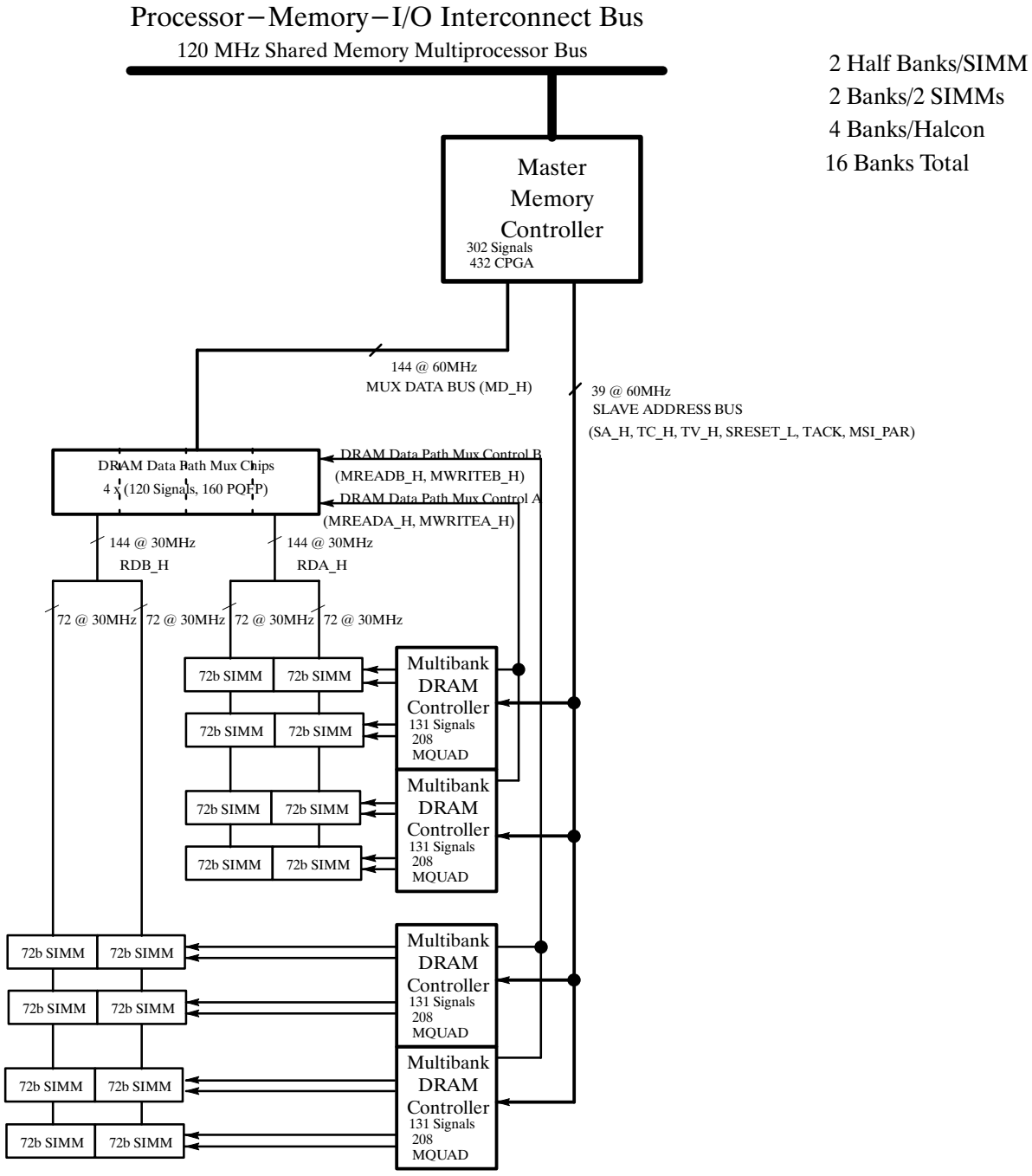

Figure 3–1. Memory System Block Diagram

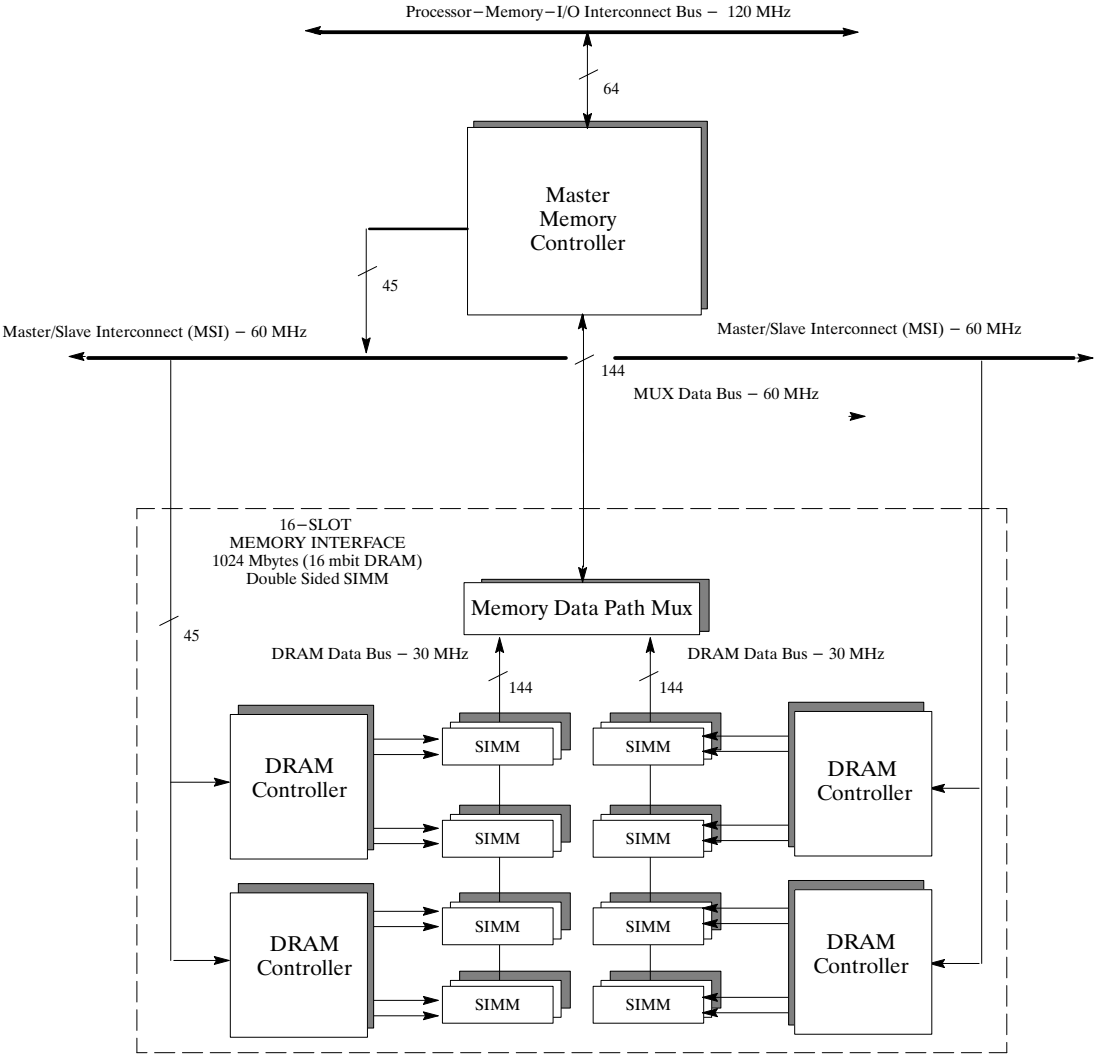

Figure 3–2. J Class Memory System

Master Memory Controller

The master memory controller is the primary interface between the interconnect bus, the system backplane, and the memory array. It helps manage the processor–memory–I/O interconnect bus protocol, including cache coherency and arbitration, provides the programmatic interface for system memory, generates and checks memory ECC, provides buffering of memory write and read transactions from the interconnect bus to the DRAM Controllers, and provides the primary high–speed memory data path to the interconnect bus. It is implemented in a 432–pin CPGA and operates most of it's internal circuitry at one–half the interconnect bus frequency – the interconnect bus interface operates at 120 MHz (nominal.)

Multibank DRAM Controller

The multibank DRAM controller provides the next level of control in the memory hierarchy, directly controlling the operation and timing of the DRAMs. Each controller (four are used) – is capable of supporting four independent, 16–byte wide banks of memory. Each bank of memory is used to assemble a 32–byte cache line using a Fast Page Mode DRAM cycle. This produces a data rate of 12 MHz (15 MHz using EDO DRAM) per 32–byte cache line, or 384 MB/sec (480 MB/sec using EDO DRAM), per DRAM Data bus. Each controller is responsible for tracking the progress of other controllers in the system for the purpose of scheduling the DRAM Data bus and MUX Data bus usage.

DRAM Data Path MUX

The DRAM Data Path MUX is the simplest of the memory components, in that its primary logic function is to combine two 144–bit DRAM Data paths into a single, 60 MHz, 144–bit MUX Data bus connected directly to the master memory controller. Additionally, it buffers the DRAM Data busses so that expansion beyond eight SIMMS may be accommodated. The DRAM data path MUX coalesces SIMM Data from two DRAM Data busses and transfers it to the master memory controller, 16–bytes at a time, at a rate of 60 MHz, or the equivalent of 768 MB/sec (960 MB/sec for EDO DRAM).

SIMM

The SIMM contains 36 DRAMs, 18 per side, with each side forming a 72–bit data word. It contains no active elements other than the DRAM. Each half is independently controlled by one of the multibank DRAM controller's four bank controllers through separate Address, RAS, CAS, OE, and W signals.

Memory Banks

The design supports from one to 16 independent banks of memory. Each bank consists of a 16–byte wide array of memory which is accessed using a page–mode cycle to fetch out 32 bytes of data (cache line). The memory bank depth is a function of the DRAM density and its organization (for example, 16Mbit x 4, 8Mbit x 8).

Multiple, parallel banks of memory are used collectively to produce very high data throughputs. Each individual bank is capable of producing 192 MB/second (213 MB/second for EDO DRAM). When combined, the banks can reach as high as 768 MB/second (960 MB/second for EDO DRAM which is the limit of the memory system). This maximum limit is primarily a function of the bank cycle time, the MUX Data bus speed – between the Master Memory Controller and the DRAM Data Path MUX (60 MHz, 16 bytes in width), and the rate transactions are issued to the memory bank controller from the master memory controller (32 byte transactions @ 30 MHz).

Sequential Address Interleaving

The memory system uses sequential address interleaving, implemented in each memory bank controller, to reduce the probability of memory bank address and DRAM Data bus contention. As more banks of memory and more busses are added to the system, the probability of contention, for both banks and busses, decreases.

Depending on the number of memory SIMMs installed, the number of interleaved banks varies. The minimum configuration interleaves two banks, while the maximum configuration interleaves 16 banks. The interleave is a function of the highest power of 2 contained within the number of installed SIMMs. If, for instance, ten SIMMs are installed, the memory system would partition that memory into eight equal sections, for an 8–way interleave. Interleaves of two, four, eight, and 16 are supported.

System Configurability

The memory system addresses a wide range of performance and cost design centers. J Class workstations nominally support a 1024 MB (max) memory configuration (using 16 Mbit DRAM). It consists of the master memory controller, four multibank DRAM controllers, one data MUX (implemented with four data MUXes), and between two and 16 SIMMs. It interleaves up to 16 banks of memory on two independent DRAM Data busses, and is limited to 768 MB/second (960 MB/second with EDO DRAM). This configuration is primarily intended for use in higher performance applications requiring large amounts of memory bandwidth.

Typical Configurations and SIMM Sizes

Memory is expanded in increments of SIMM pairs. Each SIMM pair forms two independent memory banks. Depending on the DRAM technology, the SIMM capacity varies significantly. These are two currently supported SIMM types used in all of the system configurations:

- 16 MB – 1M x 4 DRAM (4Mbit)
- 64 MB – 4M x 4 DRAM (16Mbit)

Performance and Interleaving Memory SIMMs

Note: Interleaving is only performed across SIMMs of the same size. To get the best memory performance, load SIMMs of all the same size.

When SIMMs of different sizes are installed in a system, use the following guidelines:

1. Load SIMM pairs of the same size starting from SIMM pair 1 to SIMM pair x, starting with the larger size SIMMs first.
2. Load the next pair of SIMMs (of a different size) into SIMM pair x+1. This results in both size SIMMs being evenly distributed over both DRAM busses for maximum memory bandwidth.

Note: If the total number of SIMM pairs for different size SIMMs is not the same, you may see memory performance degradation for a given application from one run to the next if the application uses memory with less banks than the previous run.

Any combination of memory may be used, although for maximum performance, we recommend using common–sized memory boards; either all 32 MB or 128 MB board pairs. To achieve both maximum performance and maximum future capacity, use 128 MB board pairs exclusively.

Figure 3–3 shows the loading order.

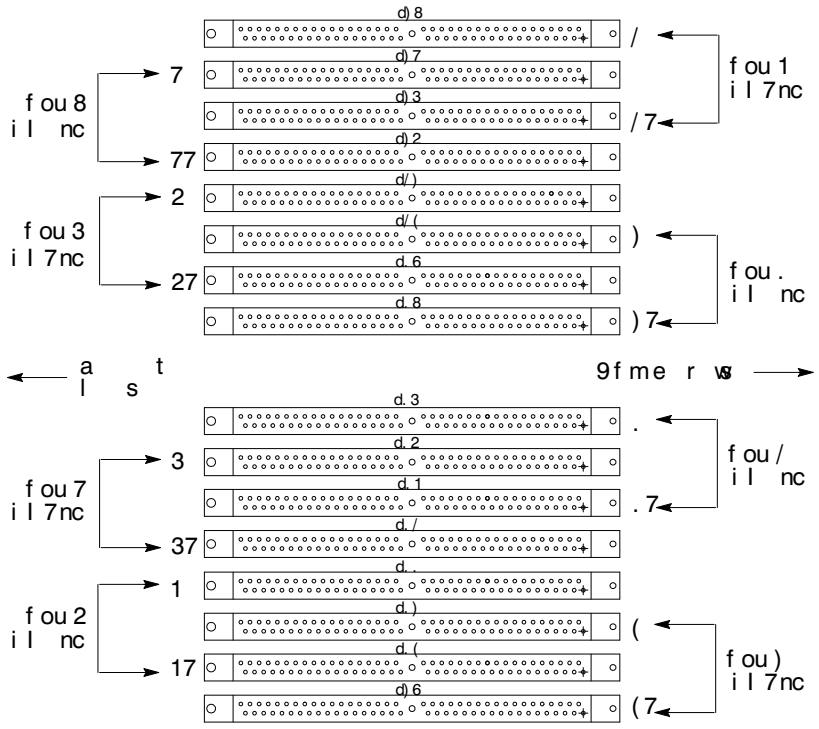

Figure 3–3. Memory SIMM Loading Order

Memory Transaction Behavior

The memory system is a large, multistream, pipeline decoupled by queues at critical points. Transactions are buffered at several points within the Master Memory Controller and the multibank DRAM Controller. Figure 3–4 shows a diagram of queue positions, as well as idle issue rates and idle latency for each component in the memory system.

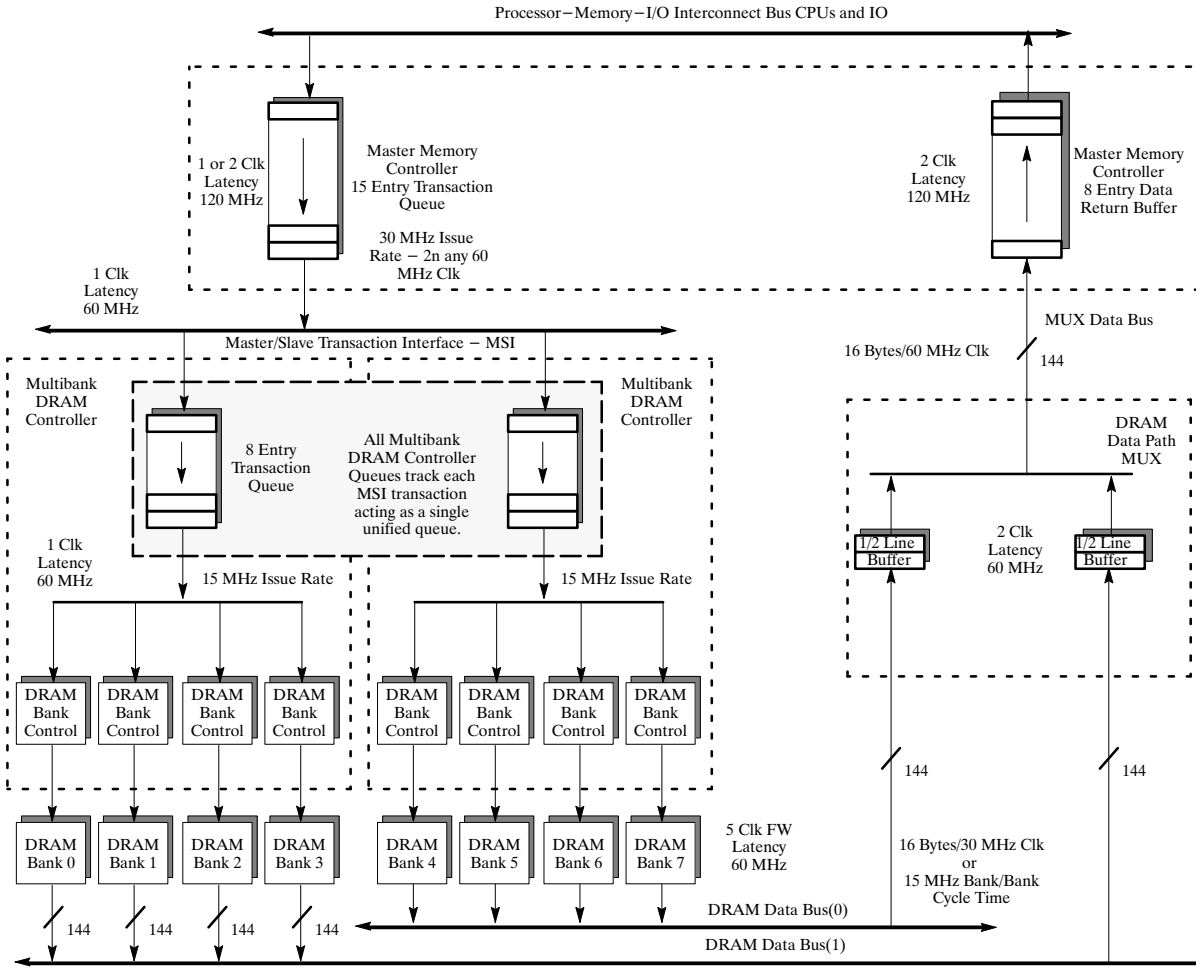

Figure 3–4. Memory System Queuing and Staging Points

Memory Queuing

Each individual multibank DRAM Controller has its own queue. However, all multibank DRAM Controller queues operate in synchronous harmony, with each multibank DRAM Controller tracking the progress of others through its own queue. In essence, they appear as one. This implementation greatly simplifies the Master/Slave Interface (MSI) protocol, but constrains transactions to execute in exact order.

The memory system has a finite limit on the number of transactions that can be queued for service at any one time, either in the Master Memory Controller or multibank DRAM Controller. The memory design, the Master Memory Controller in particular, can limit this number by either the number of CPU Cache Coherence queue entries (limited to 10) or by the number of memory queue entries (limited to 15).

Memory Transaction Pipeline

Transactions received by the Master Memory Controller from the Processor–Memory–I/O Interconnect bus, initiated by either a CPU or IO system, are passed over the MSI to each of the multibank DRAM Controllers. In an idle system, a transaction is issued beginning on any 60 MHz clock edge. Once a stream of transactions start, the Master Memory Controller issues them at a rate of 30 MHz – another design simplification.

When a transaction is received by the multibank DRAM Controller, it immediately begins a memory bank operation. The only circumstances preventing this are a refresh cycle being in progress, or a previous transaction that has not yet completed for that memory bank. Figure 3–5 depicts the transaction flow through the multibank DRAM Controller pipeline, showing that maximum throughput can result from the overlap of multiple memory banks and busses. This 768 MB/second (960 MB/second for EDO DRAM) rate is possible when transactions can be aligned to idle DRAM banks and available data "slots" on the DRAM Data busses.

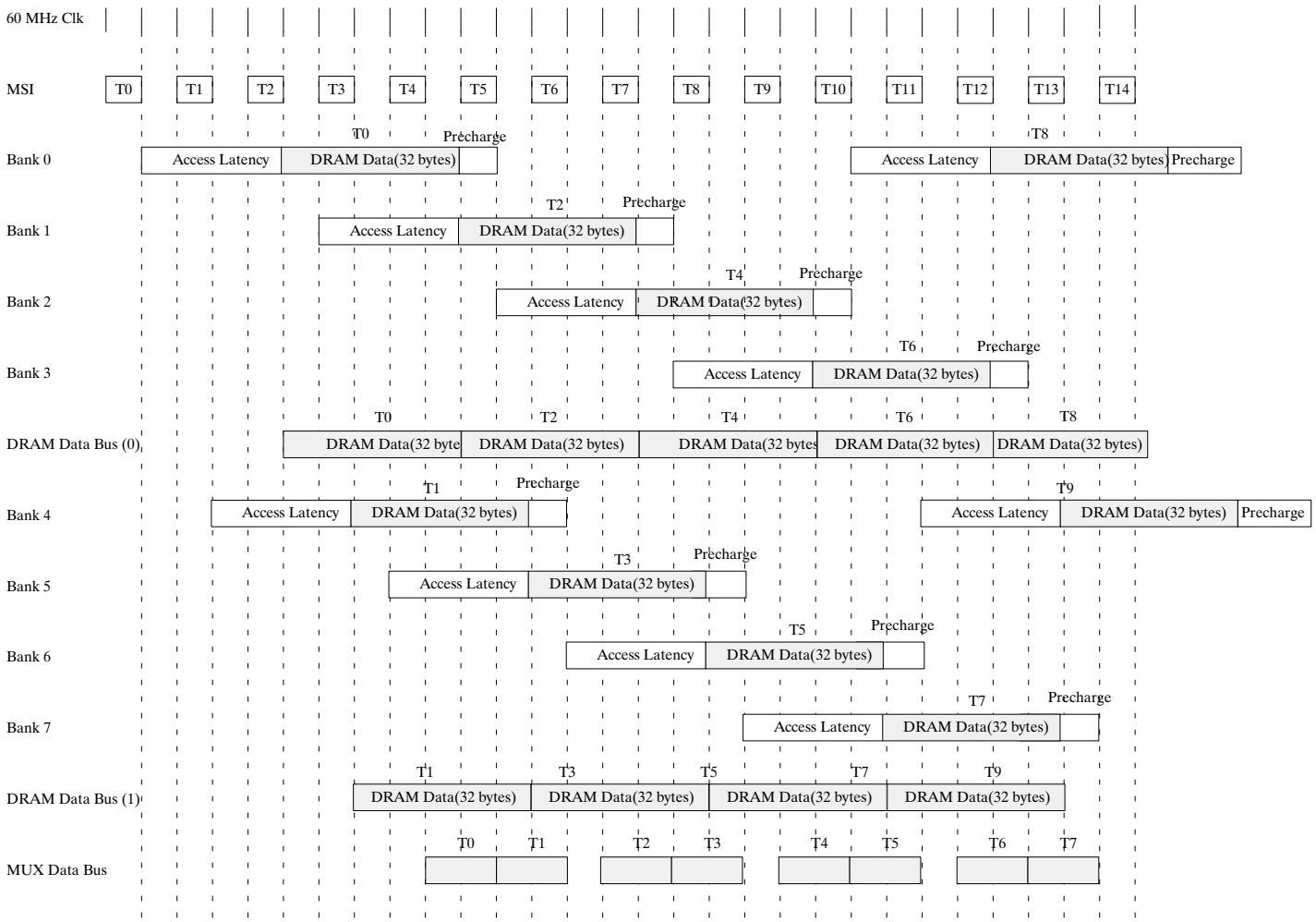

Figure 3–5. Pipelined transaction flow – 768 MB/s (Fast Page Mode DRAM)

Figure 3–5 demonstrates the top–end performance potential of the memory system. Figure 3–6 shows the counter example of performance when each memory transaction maps to the same DRAM bank address. In this case, each subsequent transaction must wait for the prior transaction to complete before it can be issued. These pipeline stalls result in a cycle time that is much greater than the fully pipelined case shown in Figure 3–5.

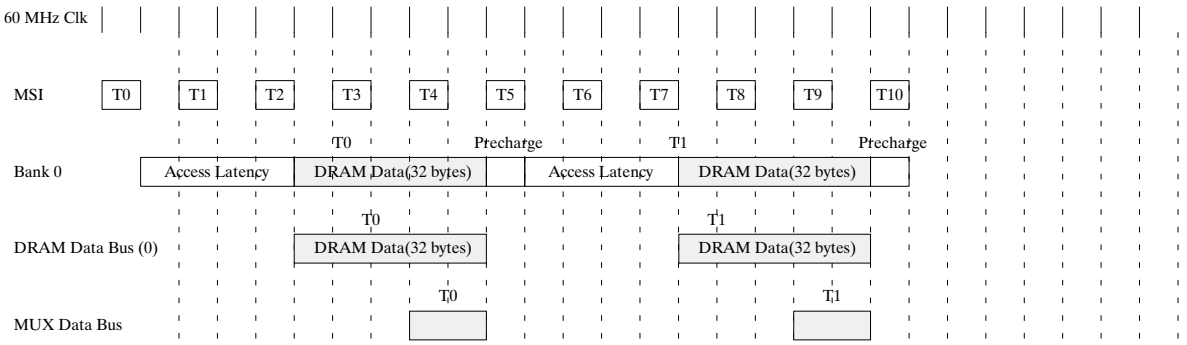

Figure 3–6. The Stalled Pipeline – 192 MB/s (Fast Page Mode DRAM)

Performance Considerations

Figures 3–5 and 3–6 show the boundaries of memory system performance with respect to cycle time or bandwidth. In reality, the cycle time will lie somewhere in between these two points. Additionally, these factors contribute to "busy" system latency, which is the latency observed when the memory system is working to satisfy the bandwidth demand.

Resource Contention

Figure 3–6 shows the behavior of the memory system when multiple transactions contend for usage of the same memory bank. In this example, the bandwidth is limited to the cycle time of a single bank of memory (a behavior exhibited by most memory systems.) In J Class systems, this behavior stalls the pipeline, resulting in a lose of parallelism. As parallelism is lost, performance is likely to degrade. The two primary factors affecting the memory system's ability to execute transactions in parallel are memory bank contention and DRAM Data bus contention.

Memory Bank Contention

Memory bank contention results from two memory transactions contending for usage of the same memory bank. Under this circumstance, the losing transaction, or second one in, is delayed until the prior transaction completes. Because transactions are constrained to complete in exact order in the design, all subsequent transactions are effectively delayed as a result of prior transaction contention.

Memory Bus Contention

Memory bus contention exhibits much the same behavior as memory bank contention, except that it results from two memory banks attempting to use the same DRAM Data Bus time "slot." The term "slot" refers to a 5 clock (4 clocks for EDO DRAM) period of time that a bank must reserve on the DRAM Data bus in order to return data to DRAM Data Path MUX. As with bank contention, this condition also causes a delay in returning data.

Estimating Memory Performance

The memory system contains one or more banks of DRAM in which each bank is 32 data bytes wide. The rate at which a single bank can be cycled is called the "bank cycle time" and is limited by DRAM technology and the timing specs for driving address and control information to the DRAMs. Currently, the implemented bank cycle time is 166.7ns for reads (150ns for reads from EDO type DRAMs) and 200.0ns for writes.

The theoretical maximum bandwidth available from multiple banks is just the sum of the bandwidths available from each individual bank. Table 3–1 summarizes the maximum DRAM bandwidth as a function of the number of banks.

Table 3–1. DRAM Bank Bandwidth

Number of Banks	Bandwidth 100% reads	Bandwidth J200 and J210 50% reads 50% writes	Bandwidth J210XC 50% reads 50% writes
1	192MB/s	176MB/s	183MB/s
2	384MB/s	352MB/s	366MB/s
3	576MB/s	528MB/s	549MB/s
4	768MB/s	704MB/s	731MB/s

Table 3–2. DRAM Bank Bandwidth for EDO DRAMs

Number of Banks	Bandwidth 100% reads	Bandwidth J200 and J210 50% reads 50% writes	Bandwidth J210XC 50% reads 50% writes
1	213MB/s	187MB/s	192MB/s
2	427MB/s	374MB/s	384MB/s
3	640MB/s	560MB/s	576MB/s
4	853MB/s	747MB/s	768MB/s

Table 3–2 shows the maximum theoretical bandwidth available from a given number of DRAM banks. The actual bandwidth provided depends on the interleaving algorithm and the access patterns. For example, although four banks can provide more bandwidth than a 120 MHz bus, performance for some applications on some systems improves if more banks are added (due to fewer bank collisions).

Workload Variance on Performance

The J Class memory system performs at its best when the memory reference pattern takes advantage of the sequential cache line interleave. In essence, strides that place subsequent references on sequential cache lines will minimize the potential for bank conflicts and maximize the memory system's throughput. The worst performing reference pattern is one that has a stride equivalent to the number of memory banks, causing each reference to continually map to one particular bank. Most other patterns fall into the random, uniform access case shown here. This modest approach to understand the memory system behavior is simply to help appreciate the effects of increasing the number of memory banks and busses for certain types of transaction behavior. It is by no means exhaustive.

Several methods exist to more accurately model the behavior and performance of a particular system design for anticipated workloads. These range from all encompassing trace–driven simulations, to simple stochastic process, Markov Chain, analytical models. These abstractions of the actual design attempt to account for the many subtle interactions present amongst the various interconnected components that otherwise would go unnoticed. Trace driven simulations run workloads derived from actual application segments on behavioral models representative of the system design. Analytical models however, use statistical probability queuing models to help understand the behavior and performance of a given design. Precise system models capable of accurately predicting performance and processing power can be somewhat complex due to the large number of states generated by the acquisition and release of parallel system resources for each of the active transactions. These resources include the CPU, containing caches,

registers, internal interconnects, and execution units, system wide resources, such as processor–memory–I/O interconnect bus arbitration and cache coherency responses, and memory system resources, memory banks and DRAM Data busses.

The following behaviors are assumed to predict system performance.

- Uniform distribution of memory addresses.
- Homogeneity – Transactions arrival rate is a function of memory retirement rate and queue length.
- Transaction Flow Balance – While not true in every state, the arrival rate is assumed to closely approximate the retirement rate through the memory system.
- The system has reached a state of equilibrium: the steady–state.
- Transaction arrival is Poisson

The following analysis presumes that the memory system has the single greatest ability to limit the system's throughput and processing power. Simply, it is assumed that the CPU, and/or IO system, is constructed in a manner that it will always exceed the memory system's ability to retire transactions. Therefore, the rate at which transactions are issued is primarily a function of their rate of retirement. So, as the retirement rate increases, the rate of issue also increases. However, the average rate at which transactions arrive for service must never exceed, and should truly be less than, the average rate at which they retire for a stable queue. Still, this positions the memory system as the primary system throughput and processing power limiter.

Memory System Characteristics

Memory system performance is normally characterized in terms of average cycle time and latency. While sometime independent, they are often related. As an example, the cycle time, or retirement rate, of the memory system affects the average latency in a queued system. An increased cycle time also increases the time a transaction sits in queue, thereby increasing the time it takes to complete the transaction from the point of issue.

The simplest, and most common, tactic used in characterizing memory system performance is to state maximum bandwidth and idle system latency values. While these are important characteristics, they do not sufficiently consider enough of the important aspects affecting memory system performance. A method capturing the effects of bank cycle time, and bus cycle time, as a functions of resource contention, would be of more interest.

Transaction Behavior

As stated earlier, the transactions are assumed to be uniformly distributed throughout memory. This is a reasonable assumption for our purposes, generally predicting modest memory system performance, especially in an MP system where the locality of reference is more random compared to a uniprocessor system. However, many memory intensive workloads do actually stride, rather than wander, through memory, thereby attaining greater throughputs, often approaching the maximum the system affords.

For this modest approximation, the rate at which transactions cycle through the system is assumed to be primarily a function of the memory system's ability to retire them. The transaction cycle time of the system is assumed to be primarily a function of the transaction issue rate, which is a function of queue sizes and retirement rate. For this analysis, a somewhat loose correlation is assumed between the issue and retirement latency of a prior transaction. Therefore, the number of "live" transactions closely approximates the maximum number of queue slots available. Also, transaction flow balance is assumed, with the average issue rate closely approximating the retirement rate.

Average Cycle Time

The primary factor determining memory system throughput and latency is the Average Cycle Time (ACT), or equivalently stated E[S] (average service time), of each transaction. The memory system ACT reflects the memory bank and bus cycle time, as well as the effect of resource contention on them – which is a function of the number of banks and busses. The factors used to determine the ACT are:

Bmx – Maximum Bank cycle or Reservation time (10 clks)
B – Number of Interleaved Banks (1, 2, 4, 8, 16, 32)
b – Number of DRAM Data busses (1, 2, 4)
bmx – Maximum DRAM Data bus cycle or "slot" reservation time
(5 clks for FPM; 4 clks for EDO)
bmn – Minimum Memory system cycle time – the MUX Data bus "slot" timing (2 clks)

The average service time, or Average Cycle Time (ACT) per transaction through the memory system, can be derived from the following:

$$\frac{Bmx}{B} + \left(1 - \frac{1}{B}\right)\left[\frac{bmx}{b} + \left(\left(1 - \frac{1}{b}\right)bmn\right)\right]$$

The above formula reflects resource contention by representing it in terms of numbers of banks and busses.

Estimating Average Memory Cycle Times and Bandwidth

With a method stated for determining average memory system cycle time, the behavior of the memory system, as a function of the number of banks and busses, is plotted. Figure 3–7 shows the bandwidth range that the memory system is capable of producing for the conditions specified for Fast Page Mode DRAM. Memory Bank Contention is shown on the vertical axis with respect to clocks per data cycle (ACT) on the horizontal axis. Bus contention is also plotted on the horizontal axis. The advantage of increasing memory banks and busses are shown for the conditions stated.

Figure 3–7 shows the data cycle time versus the increasing Fast Page Mode DRAM banks and busses.

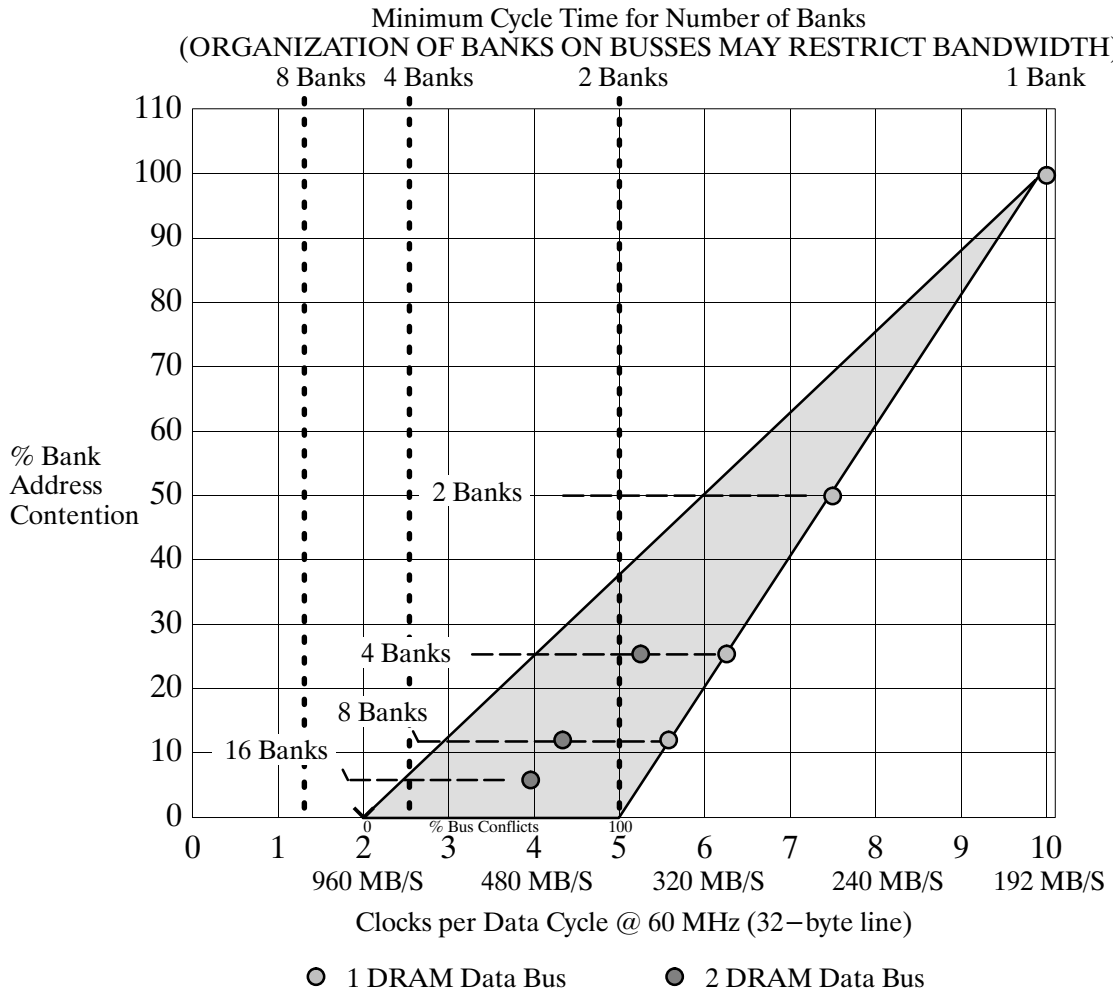

Figure 3–7. Data Cycle Time Versus Increasing Fast Page Mode DRAM Banks and Busses

Figure 3–8 shows the bandwidth range that the memory system is capable of producing for the conditions specified for EDO DRAM.

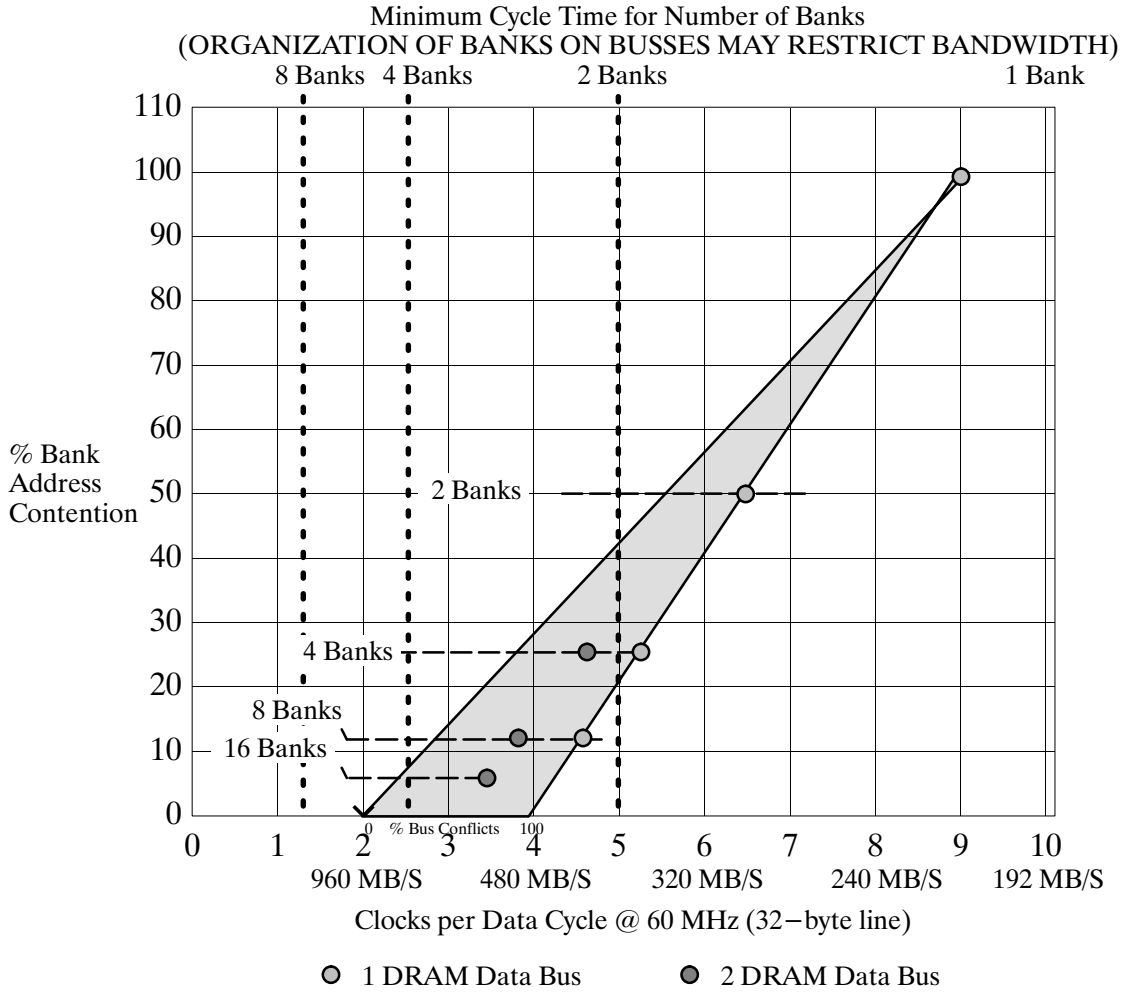

Figure 3–8. Data Cycle Time Versus Increasing EDO DRAM Banks and Busses

The above graphs characterize the J Class memory system average cycle time (ACT) and bandwidth for each of the supported configurations. The indicated data points show the effect of increasing numbers of banks and busses on memory system ACT. The two, four, eight, and 16 memory bank configurations, along with 1 and 2 DRAM Data busses, when applicable, are shown. The top horizontal axis shows the absolute minimum cycle time possible for the combination of memory banks.

It should be pointed out that the above plotted numbers do not reflect the effect of queue size and transaction time–variance on issue rate, which is a primary factor used in determining total system cycle time. To understand a closer approximation to actual system throughput and cycle time, the queue size and variance must be considered. A simple approximation can be derived from knowing the queue size and assuming Poisson transaction arrivals. This approximates the “better” case behavior of the system. Any significant work load variance is likely to degrade the issue rate beyond this point when it exceeds the benefit of the queue.

We can estimate the issue rate by knowing the ACT (*E[S]*), the average retirement rate (μ), and the average queue length (*E[N]*). The average issue rate (λ) can be derived assuming Poisson arrivals.

$$E[S] = \frac{1}{\mu}$$

$$E[N] = \frac{p}{1-p} \qquad p = \frac{\lambda}{\mu}$$

$$\frac{\lambda}{\mu} < 1 \text{ (for a stable queue)}$$

For example, the J Class design limits the number of CCC queue entries to 10. From the above formula, the average issue rate can then be determined to be 10/11, or ~91%, of the service rate. Of course these are very rough approximations.

Bandwidth Considerations

The Fast Page Mode Graph (Figure 3–6) shows a difference between the maximum bandwidth, or minimum cycle time, data points, and the calculated contention–factored data points. As shown, the largest J Class configuration, with 16 banks and 2 DRAM Data busses, produces a 4 clock per data cycle time, or 480 MB/second throughput. This example shows that memory bandwidth can be limited by two factors: bank contention and DRAM Data bus contention.

The EDO Graph shows an improvement over the Fast Page Mode configuration. The 16 bank, 2 DRAM Data bus configuration produces a 3.5 clock per data cycle time, or 540 MB/second throughput. This example shows that memory bandwidth can be improved by reducing the level of bank contention (shorter DRAM cycle time) and DRAM Data bus contention (smaller “slot timing”).

Bank Limitations

The number of memory banks significantly affects the ACT of the memory system. As more banks are added, the ACT asymptotically approaches the minimum cycle time. In general, the memory system depends on large numbers of memory banks to generate high data throughputs, via reduced bank contention.

In a typical 128 MB configuration, it is possible that only two banks of memory are available – when using 16 Mbit, 4Mbit x 4, DRAM technology. In this configuration, the memory system ACT is able only to produce 256 MB/second, which is a direct result of the small number of memory banks. This situation can be improved by using 4Mbit DRAMs instead, thereby creating four times the number of banks per MB. But this creates a potential future capacity upgrade problem and may not be cost effective in the long run.

Bus Limitations

Another factor limiting memory performance involves the small number of DRAM Data busses used. The right–most vector represents the single bus design, while the left most vector represents the best possible case with two busses.

Memory Latency Considerations

Note: This section is even more academic than the bandwidth estimations above, but included for completeness. In general, this section is simply attempting to show that memory latency is also a function of bank and bus contention, and may be improved through the addition of these resources.

Average memory latency (E[W]) can be roughly estimated using the ACT (or average service time E[S].) If Poisson transaction arrivals are assumed, then it may be found using the average issue rate (λ) and average retire rate (μ) as follows:

$$E[W] = E[N] + E[S]$$

$$E[N] = \frac{p}{1-p} \qquad p = \frac{\lambda}{\mu}$$

$$E[S] = \frac{1}{\mu}$$

$$\frac{\lambda}{\mu} < 1 \text{ (for a stable queue)}$$

Steady−State Latency

For the purpose of making some comparisons, we will define the term "steady–state" latency. The term steady–state refers to the condition when both the average issue rate and average retirement rate are constant, resulting in the average number of queued entries also being constant. Additionally, steady–state refers to a condition where there is transaction flow balance – the issue rate closely approximates the retirement rate through the system.

The value of steady–state latency is primarily a function of queue depth and the average cycle time or service time of the memory system for a given rate of contention. At this point, the latency observed at the tail of the queue is equal to the Queue depth (E[N]) * Average Cycle (Service) Time (E[S].) For an average queue depth of 10, and an average cycle (service) time of 10 clocks, one can expect that the latency for the last, or tail, transaction placed in the queue will be equal to 100 clocks.

The amount of time, or number of transactions required to reach the steady–state is a function of queue depth and the ratio of the rate transactions are put input the queue verses being extracted from it. While the average retirement rate is expected to be less than the issue rate (for a stable queue), there are periods of time when the input rate exceeds that of the output rate, thereby causing transactions to accumulate in the queue. They accumulate at a rate that is equal to the ratio of (issue/retire) – *1*. If the output rate is .2 transaction per clock, and the input rate is 1 transaction every clock, a 5:1 ratio, then 5 – 1 = 4 transactions will have accumulated in the queue for every transaction retired during that period of time.

Queue length affects system behavior in several ways. First, it determines the rate at which transactions are issued – for a fixed rate of retirement. Transaction time–variance is also a factor. If the transaction issue rate is not constant, and therefore time variant, then the queue length affects the rate at which transactions may be issued. Pulsed or clustered transactions are one example of time variant behavior, where a high rate of issue exists for short durations of time, but with an average issue rate that is generally less than the retirement rate. For a given coefficient of variance, the larger the queue, the closer the issue rate approximates the retirement rate. And, as the coefficient of variance increases, a greater queue length is required to maintain a given issue rate.

Figure 3–9 plots latency as a function of bank and bus contention for a memory system with a queue length of 10 entries, which is an average representation of the design. It is used to show that as the number of banks and busses increase, reducing the Average Cycle Time, the average latency or E[W] per transaction in the steady–state decreases.

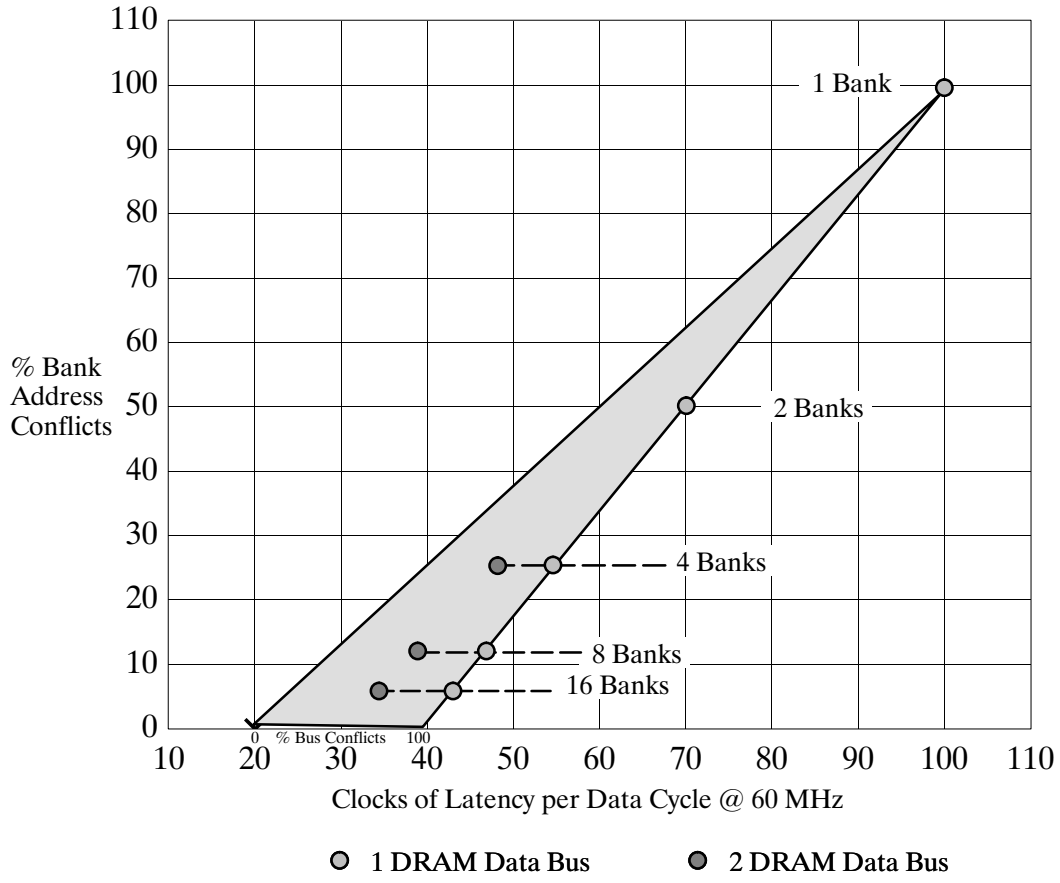

Figure 3–9. Steady–State latency for EDO DRAM
(This assumes a FULL 10 entry memory queue)

For:root
Printed on:Wed, Sep 4, 1996 12:44:56
From book:skyhawk_tech_ref
Document:ch_4
Last saved on:Tue, Mar 12, 1996 09:01:01

4

I/O System

Introduction

J Class systems support three distinct classes of I/O: namely Core I/O, Industry Standard Connectivity I/O, and high–performance proprietary I/O. Core I/O, or built–in I/O, is leveraged from the concepts of earlier workstations. Core I/O is that set of functions that are likely to be required by the majority of users, and therefore can be offered at reduced costs by removing them as options. These systems rely on EISA to serve all of the general purpose, OEM or 3rd party, connectivity I/O needs. When higher performance is needed, HP's proprietary GSC (Graphics System Connect) is available for throughputs exceeding EISA's capability.

Core I/O

The built–in, core I/O features in J Class include:

- 5 MB/sec SCSI–2; NCR53C710
- 10 Mbit/sec 802.3; Intel82596
- Centronics Parallel port
- 2 PS/2 ports for keyboard and mouse
- Stereo Audio
- RS232 (2 ports)
- HIL
- 20 MB/sec SCSI–3; NCR53C720

U2

The core of the J Class I/O system is the U2 chip. U2 connects to the CPU module via the interconnect bus and all the I/O devices via one of two GSC buses. These buses are broken down on the J Class Mother Board schematics as K0_(signal_name) and K1_(signal_name). U2 also has the EEPROM access and Real Time Clock ports. This section covers how J Class connected U2 in the system.

J Class generates its GSC buses and its Processor–Dependent Hardware I/O (PROM access and Real Time Clock ports) using the U2 chip. U2 connects the CPU–Memory–I/O interconnect with two GSC buses.

U2 incorporates two identical 32–bit GSC bus ports. Each bus port consists of 3 basic elements: the clock circuitry, arbitration logic, and the data transfer protocol logic. The clocking, arbitration, and data transfer on U2's two GSC ports are independent. U2 is the host on each of the GSC buses. U2 will master transactions directed to GSC guests operating as slaves, and will be the slave in transactions mastered by GSC guests (guest to guest transfers are not supported).

Figure 4–1 shows the J Class I/O system architecture.

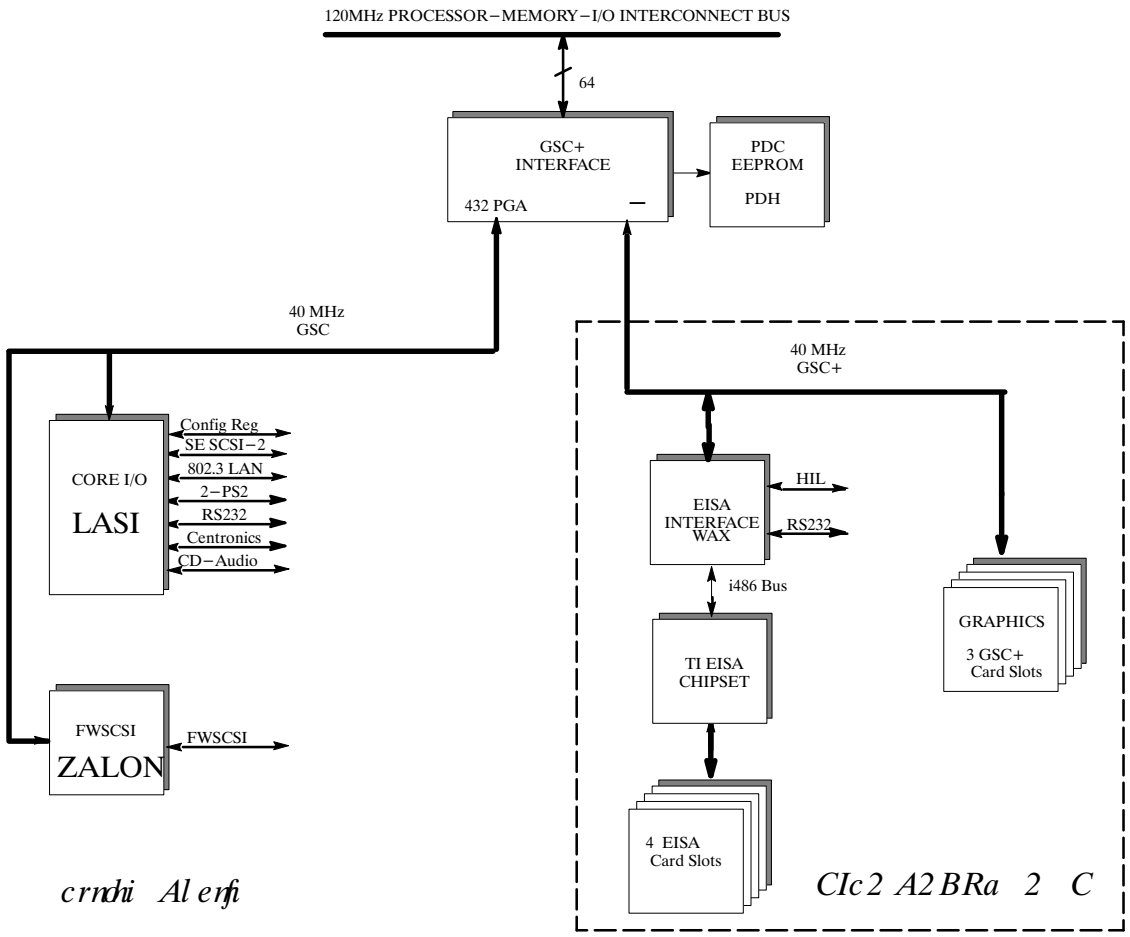

Figure 4–1. J Class I/O System Architecture

Graphics System Connect (GSC)

GSC is an interconnect consisting primarily of 48 signals, and designed to support a wide range of functions, ranging from DMA I/O devices to host manipulated graphics controllers. Some GSC features include:

GSC Features

- 32–bit shared address/data bus
- up to 40 MHz operation
- Semaphore support – Lock signal
- Address/Data bus parity detection
- Single and sub–word read/write transactions
- Multiword transactions – 2, 4, and 8 word
- Interrupt signalling – through Broadcast Interrupt Transaction
- Transaction timeouts

- DMA master support
- Sequential Transaction Request – Prefetch
- Deadlock resolution – Split signal
- Big–endian byte ordering
- Jumperless Address Space Selection
- Support for Hard Physical Addresses (HPA)
- Device HPAs
- Flex Registers
- Software Programmable Addresses (SPA)

These features allow a greater percentage of the system I/O space to be utilized, and provide an architected means for I/O expansion.

J Class uses an enhanced version of the GSC that provides the pathway for all DMA–capable I/O devices to access system memory.

Jumperless Address Space Selection has been added so that new devices can be added to the system without the need for jumpers. A Slot ID feature has been added to the GSC hardware definition to allow for up to 16 GSC devices per GSC bus. The inclusion of the SLOT ID accomplishes the following:

The inclusion of a SLOT ID in GSC has the benefit of allowing address space selection to be accomplished without jumper selection. Also, it is especially important to remove the possibility of duplicating address space configurations, resulting in unreliable operation.

J Class GSC

Figure 4–2 shows the EGSC card cage. GSC cards used in J Class are designed to an EISA–like form factor specification to enable the card cage to accommodate either EGSC or EISA cards.

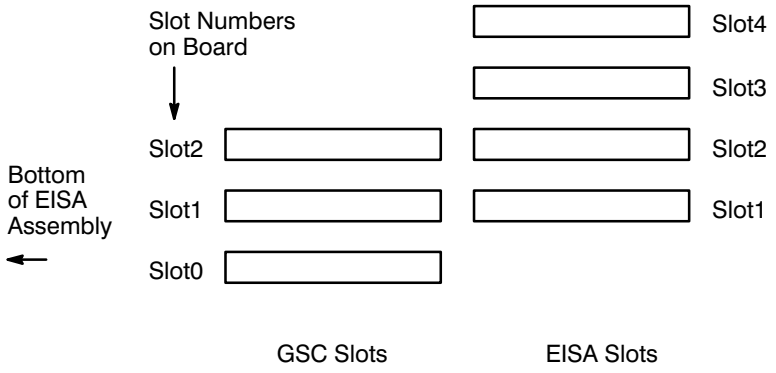

Figure 4–2. EISA/GSC Slots from Inside the EISA Assembly

Quick Reference for Parallel Slave Registers

Table 4–1 is a quick reference for the parallel slave registers.

Table 4–1. Parallel Slave Registers

Register Abreviation Name	Bit	7	6	5	4	3	2	1	0
	Bit Value	$80	$40	$20	$10	$8	$4	$2	$1
	Address*								
ParReset	slv+000	Reset (data value ignored).							
ParData	slv+800	DATA							
ParStatus	slv+801	Nbusy	Nack	pe	slct	Nerr	Nint	1	1
ParDevCtl	slv+802	1	1	NwrRd	IrqEnb	NSlin	Ninit	Autofd	Strobe
—	slv+803	Not Used (undefined)							
ModeCtl	slv+804	Mode [2]	Mode [1]	Mode [0]	Biden	fNstb	0	0	0
IECtlStat	slv+805	dmaInt	0	Nbsy-Int	Nack-Int	ack-Nbsy	peInt	slctInt	errInt
TDC0	slv+806	Timing Delay Value 0 (obsolete)							
TDC1	slv+807	Timing Delay Value 1							

* slv = 0XFFD02000

Parallel Port DMA Controller

The J Class parallel port DMA controller emulates an EISA DMA controller by providing the same register map and counter behavior. To simplify system verification and minimize area, the J Class parallel port DMA reads one 32–bit word from memory at a time and then releases the bus.

Parallel DMA Register Map

Table 4–2 shows a parallel DMA register map.

Table 4–2. Parallel DMA Register Map

DMA Controller Register Map			
Address	**Type**	**Size (Bytes)**	**Description**
[*]drst+000	write only	1	DMA Reset Register
[**]dma+000	read/write	1	Current Address Register
dma+001	read/write	1	Current Count register
dma+008	read only	1	Status Register
dma+00A	write only	1	Write single mask bit
dma+00B	write only	1	Mode register
dma+00C	write only	1	Clear byte pointer
dma+00D	write only	1	Master Clear
dma+00E	write only	1	Clear Mask register
dma+00F	read/write	1	Mask register
dma+010	read/write	1	FIFO limit register (not used)
dma+087	read/write	1	Current Address low page register
dma+401	read/write	1	High Current Count register
dma+40A	read/write	1	Interrupt Pending register
dma+487	read/write	1	Current Address High Page register

[*]drs = 0XFFD03000
[**]dma = 0XFFD01000

How Parallel Port DMA Works

The J Class Parallel Port DMA controller transfers data from memory to the parallel port without disturbing the CPU until the transfer sequence is complete. To start a sequence, the DMA channel needs to have a beginning address and byte count placed into the proper registers. Given that the mode (read or write) is set up properly, DMA will start once the mask bit is reset. After the sequence is complete, an interrupt will happen, the mask bit will be set, and the address and count registers will be at their final value. This controller does not support chaining, so after each sequence the count and address registers need to be reinitialized to their starting values.

The DMA controller does transactions by arbitrating for the bus, reading one 32-bit word, giving up the bus, and then handshaking each needed byte out to the parallel device. The DMA controller never produces multi–word GSC transactions or writes to memory.

Parity Errors and Bus Timeouts

If the J Class Parallel Port DMA controller gets a parity error or bus timeout while mastering a transaction, the transaction causing the error will be completed normally, but arbitration will be disabled so no more DMA can be done. The Current Address register will point to the next address to be read after the error. All of the data in the error transaction will be handshaked to the parallel device and the Current Count register will have the value indicating the data just read had been processed; this should help in the debug process.

RS–232 Registers

Table 4–3 shows suggested connector pinouts for the RS–232 interface. Both a nine position male D connector, such as those used in PC products, and a twenty–five position female D connector, such as those used in traditional workstations, are shown.

Table 4–3. RS–232 Connector Pinouts

Signal	Direction	9–Pin	25–Pin	Description
rs232Txd	Out	3	3	Transmit Data
rs232Rxd	In	2	2	Receive Data
rs232Cts	In	8	5	Clear to send
rs232Rts	Out	7	4	Request to send
rs232Dcd	In	1	8	Data Carrier Detect
rs232Dsr	In	6	6	Data set ready
rs232Ri	In	9	22	Ring Indicator
rs232Dtr	Out	4	20	Data terminal ready
ground		5	7	

PS2 interface

Introduction

J Class implements the keyboard and mouse interfaces as simple serial ports conforming to the de facto industry standard PS/2 specification. Each user input device has a dedicated serial port of its own. LASI includes two ports, one for keyboard and one for mouse. The interface ports rely on the software to provide all of their intelligence. Therefore, they do not interpret the characters passing through them in either direction. The interface to the host processor is through 6 one–byte registers for each port.

Registers

Table 4–4 shows the PS/2 interface registers.

Table 4–4. PS/2 Interface Registers

Register Label	Register Name	Address offset (word aligned)	Reset Value	Access
ID	ID Register	0x00	*note 1*	R
RESET	Interface reset register	0x00	0xXX	W
RCVDATA	Received data register	0x04	0xXX	R
XMTDATA	Transmit data register	0x04	0xXX	W
CONTROL	Control register—read/write	0x08	0x00 *note 2*	R/W
STATUS	Status register—read only	0x0c	0x00	R

Note 1: Each PS2 device returns a unique hardwired ID code in bits 3:0 of ID.
Note 2: Resetting the block disables it.

ID Register

Table 4–5 shows the PS/2 ID register.

Table 4–5. PS/2 ID Register

Bit	Symbol	Name	Description
3:0	ID	ID Code	Hardwired physical identification bits. (0=key-board;1=mouse)
7:4	Reserved		

Reset Register

Any write to this register will cause the interface to be reset: all buffers will be emptied and the receive/transmit state machines will be reset. The value of the data written will be discarded. Note that this does not cause the external device to be reset; it must be reset explicitly through a command sent from the host. A reset will leave the interface in the disabled state.

Industry Standard Connectivity I/O (EISA)

J Class relies on EISA to serve many I/O expansion needs. Examples of functionality available on EISA include 802.3, 802.5, FDDI, SCSI, VME adapters, X.25, Serial MUX, etc.. While the EISA specification allows for higher throughputs (33 MB/second for DMA Masters), J Class's implementation supports the more modest throughputs estimated below:

EISA DMA MASTER:
– 17 MB/sec for 32byte Master READ from memory
– 25 MB/second for 32 byte Master WRITE to memory
HOST CPU DIRECT I/O:
– 5 MB/second for 4 byte DIO READ from EISA Device
– 12 MB/second for 4 byte DIO WRITE to EISA Device

The EISA interface ASIC (WAX) is connected to the GSC bus also serving the GSC Expansion connectors in the I/O expansion card cage. In essence, EISA devices and GSC devices on the same GSC bus must share the bandwidth of the interconnect. Because it is not possible to decouple the bandwidth of the EISA and GSC devices at this time, it may be important to have the appropriate expectations regarding the distribution of GSC bandwidth if one considers using EISA for higher bandwidth applications.

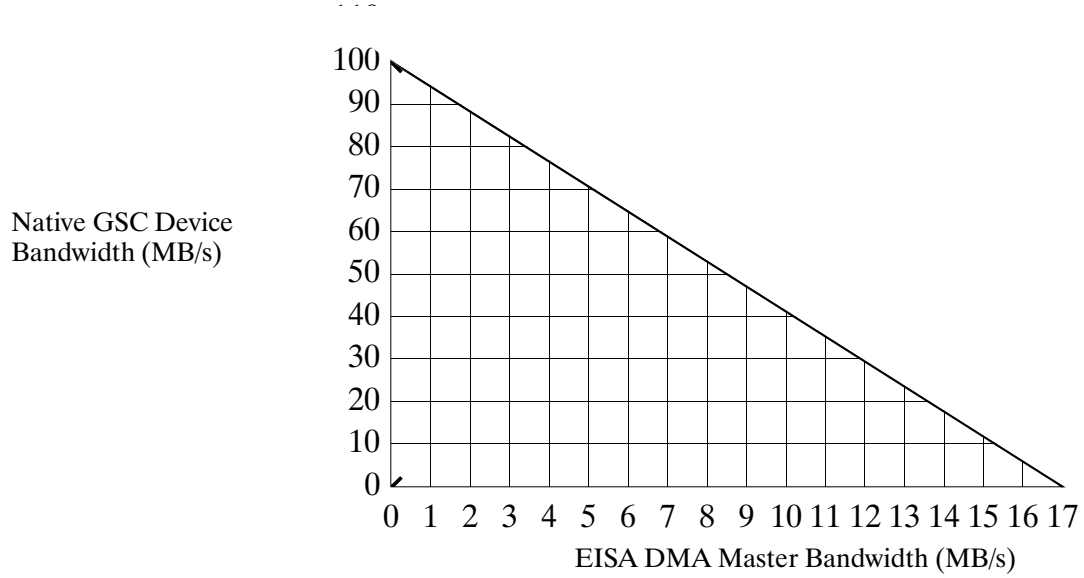

Figure 4–3. GSC Bandwidth as a Function of EISA bandwidth (Memory READ).

Figure 4–3 shows a simple distribution of GSC bandwidth based on a shared bandwidth condition involving a native GSC device and an EISA resident device. In essence, as the amount of EISA bandwidth increases, the amount of available GSC bandwidth decreases. For instance, a 10 Mbyte/s FDDI controller would consume about 60% of the total GSC bus bandwidth, leaving only 40 MB/s for a native GSC device. In general, because the EISA and GSC bandwidths are coupled, the time spent on EISA is equivalent to the time spent on GSC, but at only one fourth the throughput.

Module Overview

This module's purpose is to interface the GSC (System Connect) bus to the EISA bus, giving the system a standard expansion I/O bus. But because of EISA's complexity, this module does not directly generate EISA bus signals; it generates an i486-like bus, which the "EBCU" (EISA Bus Control Unit) and "EPCU" (EISA Peripheral Control Unit) of TI's EISA chip set then convert into EISA (and ISA). Thus, in its primary mode of operation, this is an i486 bus conversion module rather than an EISA conversion module.

Basic Operation

This conversion module supports the following functions:

- CPU reads from and writes to (E)ISA I/O addresses—also note that address scrambling is performed for accesses to *ISA* I/O space, so that each ISA board gets its own protectable page in the CPU's address space.
- CPU reads from and writes to (E)ISA memory addresses—only 55.5 MB out of (E)ISA's 4 GB address space is accessible to the CPU, but the accessible ranges include subsets of each of ISA 20-address-bit, ISA 24-address-bit, and EISA 32-address-bit memory.
- CPU reads from and writes to the address map RAM—after the CPU sets it up, this mapper lets (E)ISA master and DMA devices access any desired pages in system RAM.
- CPU reads from and writes to the Lock Control Register—this register lets the CPU run a sequence of "locked" (undivided) cycles on the EISA bus.
- CPU reads from and writes to the FIFO Enable Register—this register lets the CPU flush the inbound buffer and clear the outbound buffer, or disable data buffering altogether.
- CPU reads from the Interrupt Acknowledge Register—this is the way the CPU runs interrupt acknowledge cycles to the (E)ISA interrupt controller and obtains the "interrupt vector" number of the highest pending (E)ISA interrupt.
- (E)ISA master and DMA reads from and writes to the mapped address space—these accesses are passed through to the system RAM, after having their addresses translated by the appropriate address map entries. If these accesses are not "locked" on the EISA bus, they can be buffered: writes do not immediately occur to system RAM, and reads can be satisfied from data which was pre-fetched from system RAM. If these accesses are "locked" by the assertion of EISA's `LOCK` signal, the lock is propagated all the way back to system RAM, and no other masters can run bus cycles or access system RAM between the locked EISA cycles.
- Interrupt requests and non-maskable interrupts from (E)ISA—after flushing and clearing the data FIFO to ensure that the system sees consistent data, these are simply passed to the interrupt controller where they are dealt with appropriately.

Functional Description Block Diagram

This block diagram describes the GSC to EISA Interface.

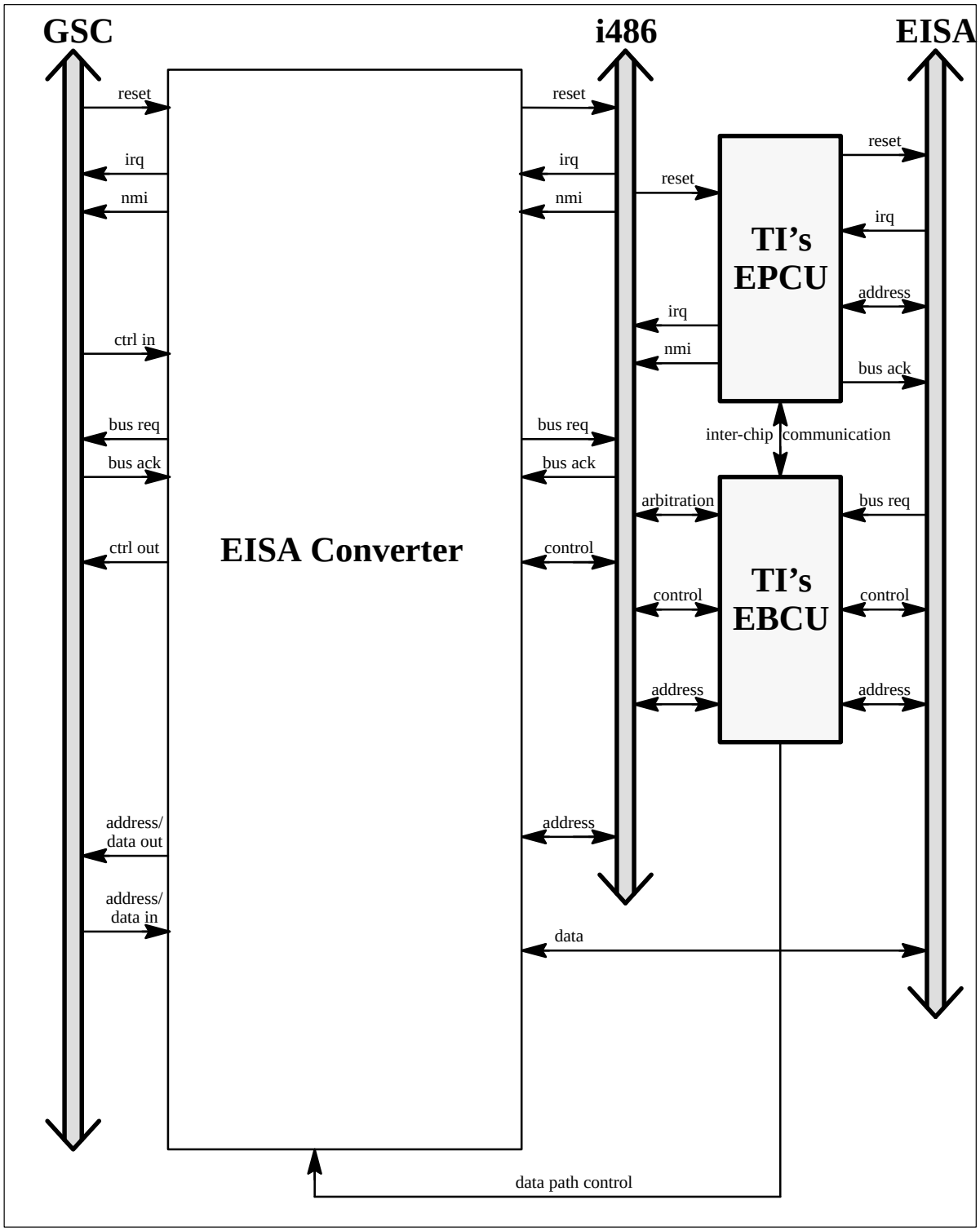

Figure 4–4. GSC to EISA Interface Block Diagram

Figure 4–5 shows the converter's address space as seen *by the CPU*.

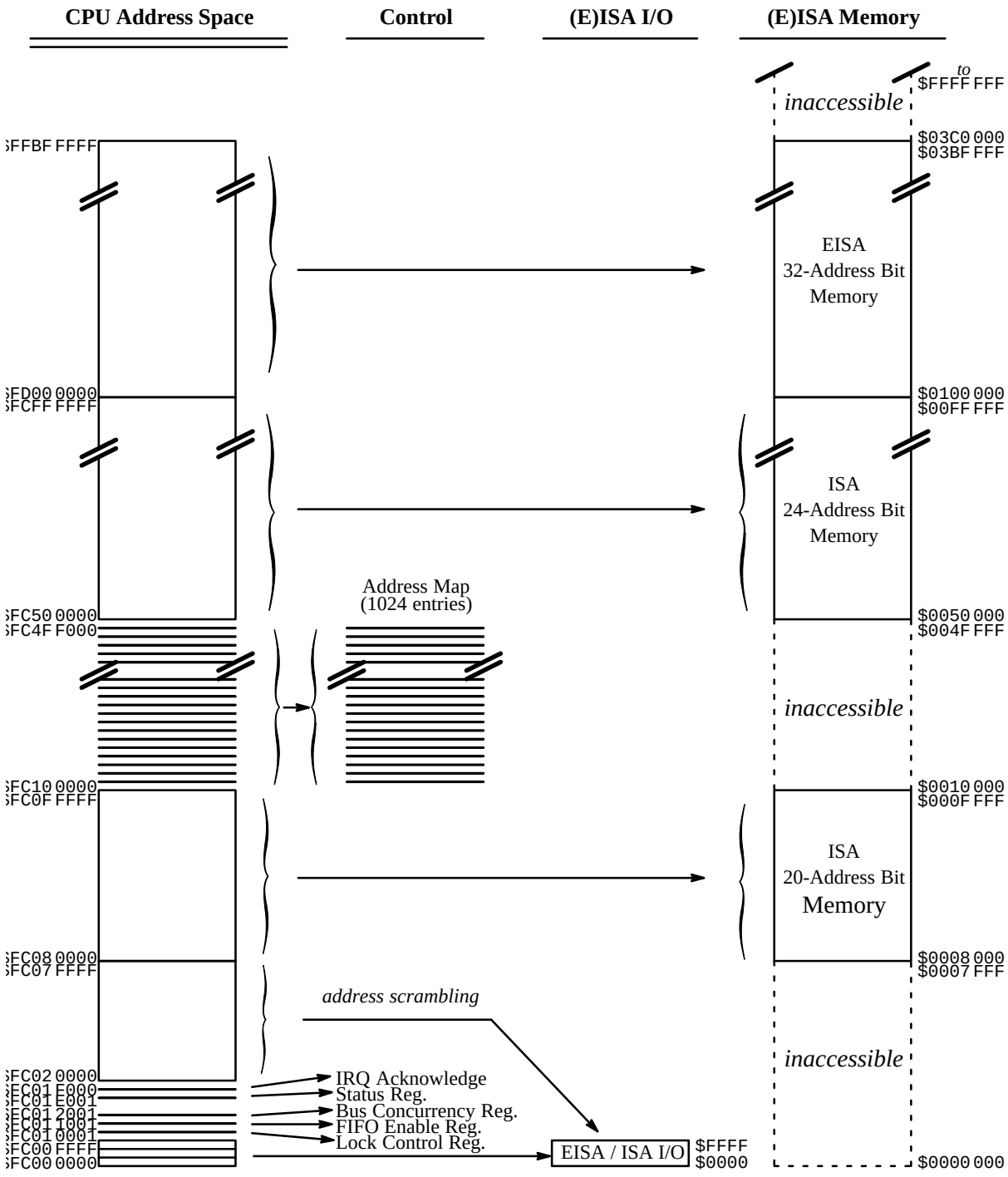

Figure 4–5. Accesses from the CPU

Figure 4–6 shows (E)ISA *memory* space as seen *by an EISA or ISA master*

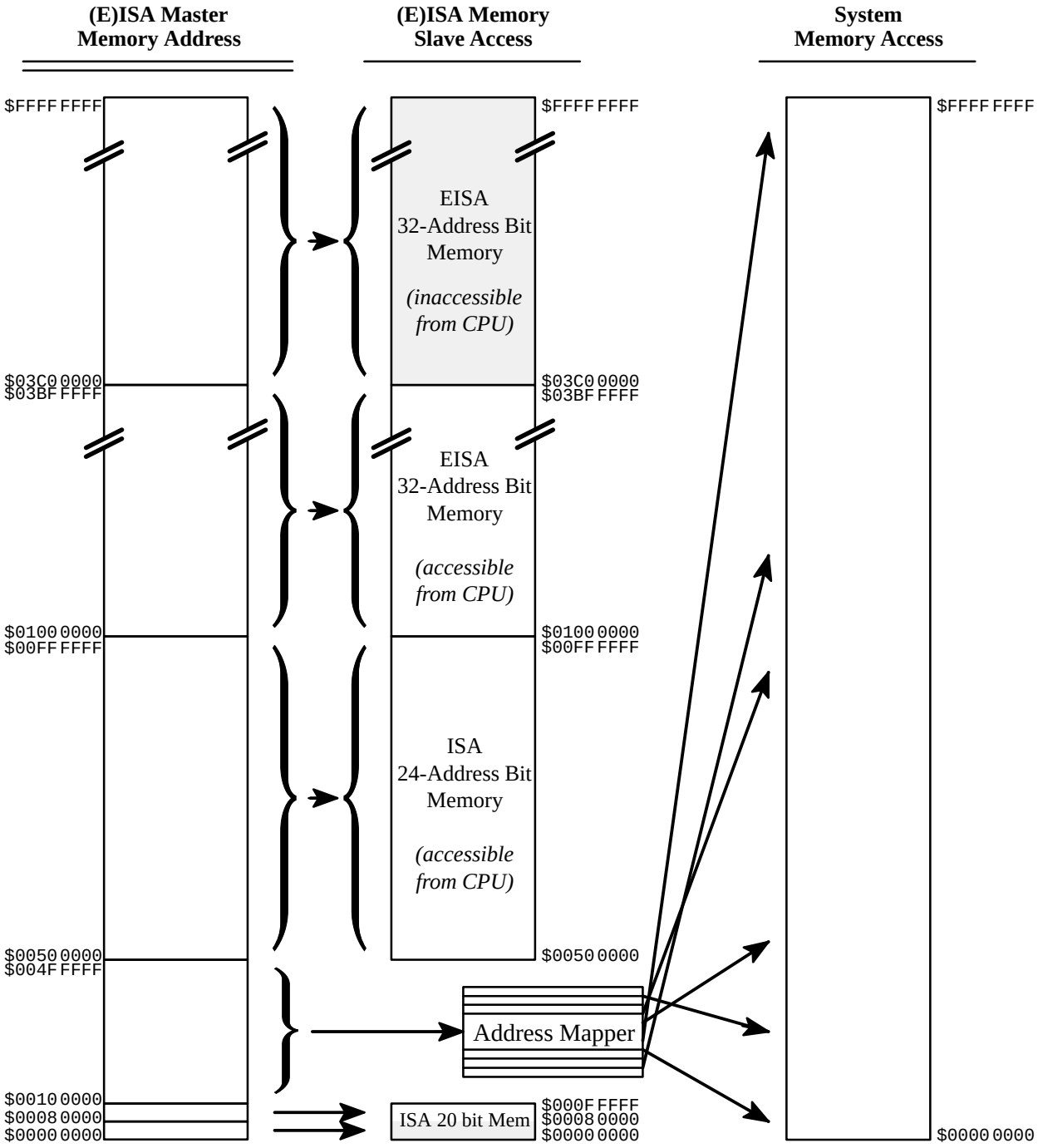

Figure 4–6. Accesses from an EISA Master

Unsupported EISA options

Besides the list of HP supported option cards above, you can install other EISA or ISA board designs. The EISA bus on J Class is an industry standard EISA as implemented by the TI chipset. See the appropriate chip data sheets for more information. Also, be aware that adding boards can introduce hardware problems which must dealt with separately.

Graphics

Table 4–6. Multi–Head Graphics Test and Support Matrix

Heads	Color Graphics	Dual Color Graphics	HCRX or HCRX24	HCRX–Z HCRX24Z	CRX48Z
1	1				
1			1		
1				1	
1					1
1					
2	2				
2		1			
2			2		
2	1			1	
2	1				1
3		1	1		
3		1		1	
4		2			
This matrix ensures that at least one GSC slot remains free for non–graphics use.					

Audio Subsystem

J Class provides stereo quality audio output with a 16–bit codec. The codec combines quality stereo A/D converters for microphone and line input levels, as well as D/A converters for driving headset and the speaker. The input sampling rate and format are programmable, as are the input gain control (used for software control of recording levels) and output attenuation.

The output is capable of driving 8 Ohms, it can also be used for higher impedance devices with little or no additional distortion, thus a line level input can be driven by the headset output. The input and output specifications are found in Chapter 1 of this book.

PDH subsystem

The Processor Dependent Hardware subsystem is the hardware that supports the PDC(firmware) in the J Class system. There are two main parts of the PDC, the Flash PROM and Scratch RAM. Scratch RAM is used by both the PDC and the Operating System to store run–time information. The Flash PROM provides storage of PDC code which is the start–up code that runs the system.

The PROM consists of two 512k x 8 Flash PROMS, which are addresses sequentially, to provide 1Mbyte of storage space for this code. Both the parts used are of AMD AM29040–120JC type. The in–circuit programming of these parts is controlled by the U2 chip, and updates are performed by a software “update” program which can be run off a tape drive or over the LAN.

The Scratch RAM is a 32k x 8 SRAM, PN HM62256ALFP–101. This again is controlled by the U2 chip, and can be written to by either the firmware, or the Operating System directly.

Another part of the PDH system is the LCD. This is a 2–line x 16 display that PDC and the OS uses to display data to the user of the system. Since there is only a power LED on the system, this display panel is the basic vehicle to return data, messages, and error messages to the user.

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Document:ch_5
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5

Internal Mass Storage

SCSI Bus

Table 5–1 lists recommended SCSI mass storage device bus addresses. Mass storage device upgrades have these addresses factory set.

Table 5–1. Recommended SCSI Addresses

Unit or Mass Storage Device	Recommended Bus Address
SCSI host controller	7
First Hard Disk Drive	6
Second Hard Disk Drive	5
DDS Tape Drive	3
CD ROM Disk Drive	2
SCSI Floppy	0

SCSI circuits must have terminating resistors installed on them. The two configurations are terminated as follows:

- When using the external SCSI configuration, you must use an active SCSI terminator at the last external device on the SCSI bus.
- All other devices, external or internal, must not be terminated.
- Use only HP K2291 terminators to ensure reliable system operation.

Note Consult the documentation that accompanies each SCSI device for specific information concerning its use. Refer to Appendix C of the *J Class Owner's Guide* for information about connecting SCSI devices to the workstation.

Hewlett–Packard only supports SCSI devices that were designed for the J Class workstation. Third–party SCSI drives are not supported, but if they meet SCSI–II specifications, they should work on the J Class workstation. These third–party devices may not perform as well as supported drives, due to special firmware (such as write caching) in the J200 SCSI drives that optimizes I/O performance.

Internal storage devices supported are:

- Fast, Wide SCSI Hard Disk Drives – up to two:
  1.0 GB Drive
  2.0 GB Drive
- Single–Ended SCSI Removable Media – up to two
  CD–ROM Drive
  4.0 GB, 4–mm DDS Tape Drive
  SCSI Floppy Drive

Refer to Chapter 1 for the list of magnetic media devices supported.

See Chapter 9 for information on the fast, wide differential drive connector pinnouts.

Electrical Information

Power Requirements

Table 5–2. Mass Storage Power Requirements

Voltage	2 GB	1 GB	Floppy Drive
+5 V	1.55A	1.15A	0.8A ave.
+12 V	1.7A	0.8A	0.3A ave.

Connector Pinouts

Table 5–3. SCSI Interface Signals

Pin No.	Signal	To	Description
02	DB[0]	B	Data Bus (LSB)
04	DB[1]	B	Data Bus
06	DB[2]	B	Data Bus
08	DB[3]	B	Data Bus
10	DB[4]	B	Data Bus
12	DB[5]	B	Data Bus
14	DB[6]	B	Data Bus
16	DB[7]	B	Data Bus (MSB)
18	DB[P]	B	Data Bus Parity
20			
22			
24			
26	Termpwr	B	Terminator Power
28			Reserved
30			Not Used (GND)
32	ATN	D	Indicates message available for drive
34			Not Used (GND)
36	BSY	B	Signal indicating bus is in use
38	ACK	D	Data/Command transfer handshake
40	RST	D	Or–tied signal indicating reset condition
42	MSG	H	Indicates message phase
44	SEL	B	Signal indicating selection/reselection phase
46	C/D	H	Indicates whether control or data information is on data bus
48	REQ	H	DataCommand transfer handshake
50	I/O	H	Indicates direction of information transfer. Assertion indicates transfer to host.

H = Host D = Drive B = Bidirectional

Note All odd pins are signal returns and must be connected to signal GND at the drive, except pin 25 which is left free to protect against misinsertion.

Termination Strategy

Any single–ended standard SCSI–2 device connecting to the system board must use a 50–pin high–density thumb screw connector on the end connecting to the system board, and a 50–pin low–density bail lock connector on the other end. If you attach a second SCSI–2 device, the cable must have low–density connectors on each end.

Any fast, wide differential SCSI–3 device connecting to the system board must use a 68–pin high–density thumb screw connector on both ends.

The last device connected to the SCSI bus must be terminated with a SCSI terminator. All of the devices listed ship without terminators. If you do not already have a SCSI terminator, you must order terminator K2291 (for 50–pin connectors) or C2905A (for 68–pin connectors) from Hewlett–Packard.

Note: When attaching external SCSI devices, be sure to terminate the last device on the external SCSI bus. If no external devices are attached, the SCSI connector on the rear of the system must be terminated with the terminator that was shipped with your workstation.

Figure 5−1 shows a J Class workstation with the SCSI terminators attached.

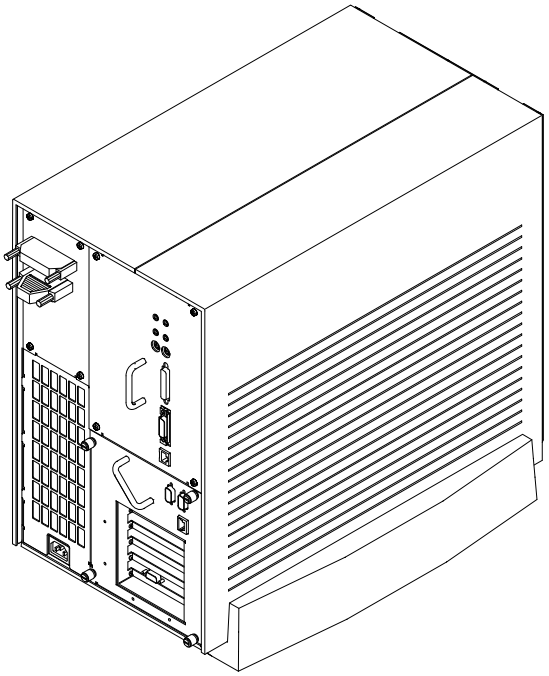

Figure 5–1. Rear Panel SCSI Connectors with Terminators Attached

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Packaging

Shipping Carton

Box Specifications

1. 500 PSI 33 lb high ring crush liner board. Double wall corrugated.
   Half slotted carton design.
2. Color: Kraft
3. Interior Dimensions: L – 28.25 inches, W – 17.75 inches, D – 23.625 inches
4. Closure: Outer stitched seam
5. Markings: Print with ink to match GCMI No. 31 Blue
   Print per photomasters: 5955–6670 HP company logotype 12 1/2 inches
   5955–6677 ISO Symbols – Vertical
   5955–6673 Environmental statement
   5955–6691 Lifting Limitation Graphic (100 lbs, 45 kg)
   016691 Open Me First
   A1630–84023–2 Install. Instruct. Encl.
   A1658–84011–2 Disk Drive Warning
   A1658–84021–2 CE Mark (no year indicated)
   AW–A1658–84037–11 AW–PA RISC Powered (size 130%)
   AW–A1658–84040–11 Unpacking Pictorial
   AW–A1658–84041–11 Label Registration

Carton Markings and Placement

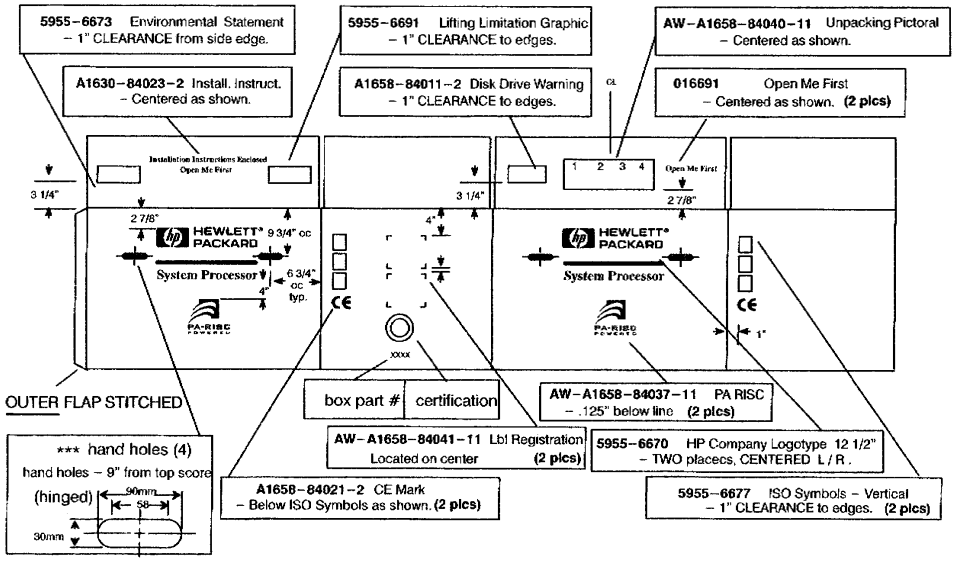
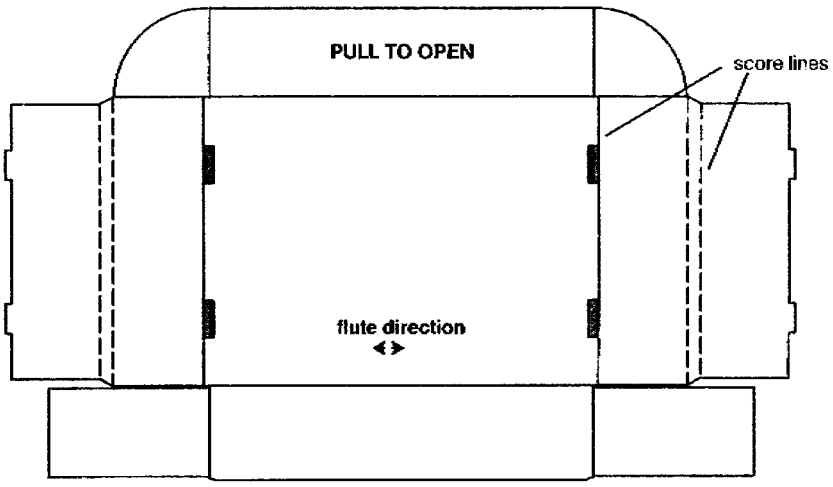

5955–6673 Environmental Statement – 1" CLEARANCE from side edge.
5955–6691 Lifting Limitation Graphic – 1" CLEARANCE to edges.
AW–A1658–84040–11 Unpacking Pictoral – Centered as shown.
A1630–84023–2 Install. instruct. – Centered as shown.
A1658–84011–2 Disk Drive Warning – 1" CLEARANCE to edges.
016691 Open Me First – Centered as shown. (2 plcs)
Installation Instructions Enclosed Open Me First
Open Me First
3 1/4"
2 7/8"
HEWLETT PACKARD
9 3/4" oc
System Processor
6 3/4" oc typ.
4"
CE
PA-RISC
xxxx
OUTER FLAP STITCHED
box part #
certification
AW–A1658–84037–11 PA RISC – .125" below line (2 plcs)
AW–A1658–84041–11 Lbl Registration Located on center (2 plcs)
5955–6670 HP Company Logotype 12 1/2" – TWO placecs, CENTERED L / R .
*** hand holes (4)
hand holes – 9" from top score
(hinged)
90mm
58
30mm
A1658–84021–2 CE Mark – Below ISO Symbols as shown. (2 plcs)
5955–6677 ISO Symbols – Vertical – 1" CLEARANCE to edges. (2 plcs)

Figure 6–1. Carton Side Panel Markings and Placement



MATERIALS

275 lb, DOUBLE WALL CORRUGATED TRAY, KRAFT COLOR

INSIDE DIMENSIONS: L–29.25" W– 18.5" D– 6"

MARKINGS: Print with ink to match **GCMI No. 31 BLUE**
PULL TO OPEN in 1/2" high letters

Figure 6–2. Package Tray – Bottom View

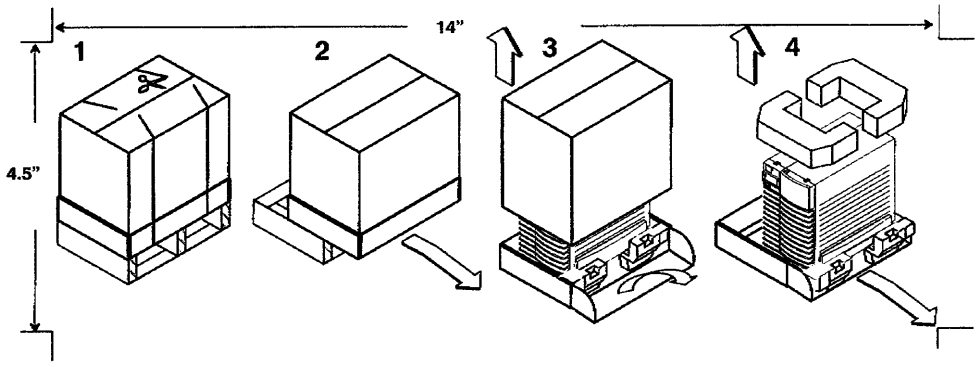


Figure 6–3. Unpacking Pictorial

r t i w
n t t d
13s 2 1c369 1 1/4 7 9/a(1
r t t t 2) e 7
63l w u t 2 76 7 1/6 7/a(1
r t t t 2) e 9
.6 u 17 /

mt 13 69(w t 3

r t w w u w t t t u t w w (
t ww ot t r t i t f wt 3

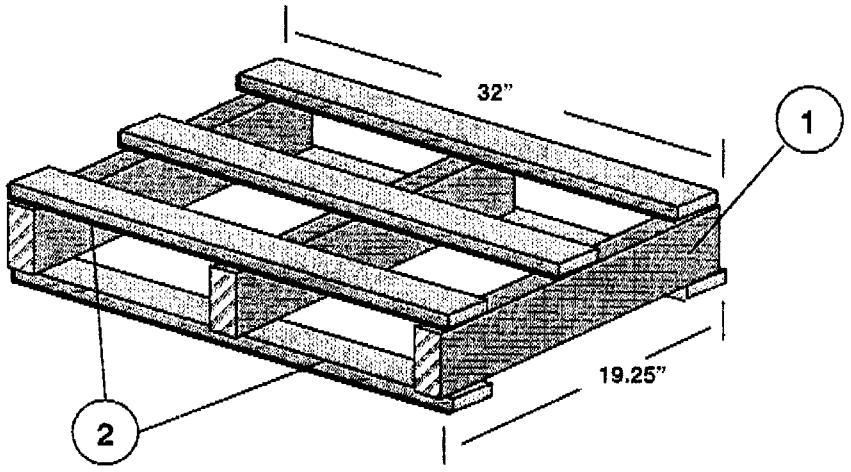


Figure 6–4. Package Pallet

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Document:ch_7
Last saved on:Tue, Mar 12, 1996 09:01:07

7

Power Supply

Functional Information

The power supply is a custom designed 484 watt switching converter with a universal AC front end operating from 120/240 V nominal source. The power supply provides five main regulated outputs: +5.1V, +4.5V, +3.4V, +12V, and –12V. It also provides one auxiliary output of +15V that is present whenever AC power is applied to the unit. The five main outputs are enabled via a PCL–L switch (remote switch). Any fault conditions that arise (for example, over current, over voltage, or over temperature) within the main power supply will cause the power supply to shutdown and latch off. The latch is removed by either cycling AC power or the PCL–L switch after the fault condition is removed.

Fans are included as an integral part of the power supply to cool the system and power supply. The system is designed so the fans provide maximum cooling with all the covers in place.

Power Supply Specifications

Table 7–1, Table 7–2, and Table 7–3, show the power supply output specifications, input specifications, and demand.

Table 7–1. Power Supply Output Specifications

	+5V (A) Main	+4.5V (A)	+12V (A)	+3.4V (A)	–12V (A)	+15V AUX (A)
Current	82.0	00.0	5.00	0.00	1.20	0.30
Condition A			(10.0A)			(fan)
Current	66.0	11.0	5.00	8.00	1.20	0.30
Condition B			(10.0A)			(fan)
Current	00.0	00.0	0.00	0.00	0.00	2.00
Condition C						

−16.5

1. The above synopsis is for reference only.
2. This power supply is enclosed and includes fans.
3. Maximum total continuous DC power is 484 watts.
4. Numbers in () are for 10 second surge.

Table 7–2. Power Supply Input Specifications

Input Power	664W
Input Voltage (115V range)	88 to 138Vac RMS
Input Current (115V range)	11.5A RMS max.
Input Voltage (230V range)	193 to 269Vac RMS
Input Current (230V range)	6A RMS max.
Line Frequency	45 to 66 Hz

Table 7–3. Power Supply Demand

System Board (Dual Processor)	203.0 W
LAN	5.0
SCSI Adapter	3.0
Multi Function I/O	2.5
RS232 & Centronics	1.5
Multimedia	4.9
HP HIL	10.0
Drives – 2 x 2 GB FW	36.8
Drive – CD–ROM	6.0
Drive – Floppy or DDS	6.0
Fans	7.2
Graphics and keyboard Interface	8.0
EISA	110.2
Total Power	**407.6 W**

Electrical Information

Output Connectors

There are three panel mount output connectors used; P1, P2, and P3.

P1 housing:	Molex 15–06–0180 (18 position)
P2, P3 housing:	Molex 15–06–0240 (24 position)
P1, P2, and P3 contacts:	Molex 39–00–0078, 16AWG or Molex 39–00–0039, 18–24AWG

For:root
Printed on:Wed, Sep 4, 1996 12:45:45
From book:skyhawk_tech_ref
Document:ch_8
Last saved on:Tue, Mar 12, 1996 09:02:21

8

Keyboard Layouts

Dimensions

The J Class workstation supports 14 different language keyboards. Each keyboard comes with a 7.5 foot mini–DIN style cable. The physical characteristics are as follows:

Length:	467 mm (18.4 in)
Width:	184 mm (7.25 in)
Height:	48 mm (1.9 in)
Weight:	1.09 kg (2.4 lb)

Japanese version:

Length:	455.7 mm (17.95 in)
Width:	164.51 mm (6.48 in)
Height:	38.07 mm (1.50 in)

Keyboard Layout

Figures 6–1 through 6–14 show the 14 keyboard key layouts available for the J Class workstations.

.050
.065
USE ITEMS 41 AND 55
FOR SETUP
3 PRINT LOCATION
Esc
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12
Print Screen Sys Rq
Scroll Lock
Pause Break
Insert
Home
Page Up
Delete
End
Page Down
Num Lock
Enter
Caps Lock
Alt
Alt Gr
Ctrl
3 USE THE "PRINT LOCATION" DIAGRAM FOR ON LINE PAD PRINT SETUP.
2. COPIES OF THE ORIGINAL DRAWING MAY BE USED AS AN INSPECTION AID FOR THE PURPOSE OF CUSTOMER APPROVAL OF THE LEGEND LAYOUT, AS WELL AS IDENTIFICATION OF KEYTOP MISLOADS OR MISLOCATED CHARACTERS ON KEYTOPS. THE TOLERANCES NOTED BELOW ARE APPLIED TO THE DRAWING ONLY. THESE TOLERANCES DO NOT APPLY WHEN THIS DRAWING IS USED FOR PURPOSES OTHER THAN THOSE LISTED ABOVE.
DRAWING ±.015 - INDIVIDUAL LEGEND LOCATION FROM PN3000 BOM.
TOLERANCES: ±.100 - DISTANCE BETWEEN REGISTRATION KEYTOPS AS NOTED IN THE PRINT LOCATION DIAGRAM (DUE TO DRAWING REPRODUCTION).

Figure 8–1. Danish Keyboard

.050
.065
USE ITEMS 41 AND 55
FOR SETUP
3 PRINT LOCATION
3 USE THE "PRINT LOCATION" DIAGRAM FOR ON LINE PAD PRINT SETUP.
2. COPIES OF THE ORIGINAL DRAWING MAY BE USED AS AN INSPECTION
AID, FOR THE PURPOSE OF CUSTOMER APPROVAL OF THE LEGEND LAYOUT,
AS WELL AS IDENTIFICATION OF KEYTOP MISLOADS OR MISLOCATED
CHARACTERS ON KEYTOPS. THE TOLERANCES NOTED BELOW ARE APPLIED
TO THE DRAWING ONLY. THESE TOLERANCES DO NOT APPLY WHEN THIS
DRAWING IS USED FOR PURPOSES OTHER THAN THOSE LISTED ABOVE.
DRAWING ±.015 - INDIVIDUAL LEGEND LOCATION FROM PN3000 BOM.
TOLERANCES: ±.100 - DISTANCE BETWEEN REGISTRATION KEYTOPS AS NOTED IN
THE PRINT LOCATION DIAGRAM (DUE TO DRAWING REPRODUCTION).

Figure 8–2. French Keyboard

.065
USE ITEMS 41 AND 55
FOR SETUP
3 PRINT LOCATION
3 USE THE "PRINT LOCATION" DIAGRAM FOR ON LINE PAD PRINT SETUP.
2. COPIES OF THE ORIGINAL DRAWING MAY BE USED AS AN INSPECTION
AID, FOR THE PURPOSE OF CUSTOMER APPROVAL OF THE LEGEND LAYOUT,
AS WELL AS IDENTIFICATION OF KEYTOP MISLOADS OR MISLOCATED
CHARACTERS ON KEYTOPS. THE TOLERANCES NOTED BELOW ARE APPLIED
TO THE DRAWING ONLY. THESE TOLERANCES DO NOT APPLY WHEN THIS
DRAWING IS USED FOR PURPOSES OTHER THAN THOSE LISTED ABOVE.
DRAWING ±.015 - INDIVIDUAL LEGEND LOCATION FROM PN3000 BOM.
TOLERANCES: ±.100 - DISTANCE BETWEEN REGISTRATION KEYTOPS AS NOTED IN
THE PRINT LOCATION DIAGRAM (DUE TO DRAWING REPRODUCTION).

Figure 8–3. German Keyboard

.050
.065
USE ITEMS 41 AND 55
FOR SETUP
3 PRINT LOCATION
3 USE THE "PRINT LOCATION" DIAGRAM FOR ON LINE PAD PRINT SETUP.
2. COPIES OF THE ORIGINAL DRAWING MAY BE USED AS AN INSPECTION AID, FOR THE PURPOSE OF CUSTOMER APPROVAL OF THE LEGEND LAYOUT, AS WELL AS IDENTIFICATION OF KEYTOP MISLOADS OR MISLOCATED CHARACTERS ON KEYTOPS. THE TOLERANCES NOTED BELOW ARE APPLIED TO THE DRAWING ONLY, THESE TOLERANCES DO NOT APPLY WHEN THIS DRAWING IS USED FOR PURPOSES OTHER THAN THOSE LISTED ABOVE.
DRAWING ±.015 - INDIVIDUAL LEGEND LOCATION FROM PN3000 BOM.
TOLERANCES: ±.100 - DISTANCE BETWEEN REGISTRATION KEYTOPS AS NOTED IN

Figure 8–4. Italian Keyboard

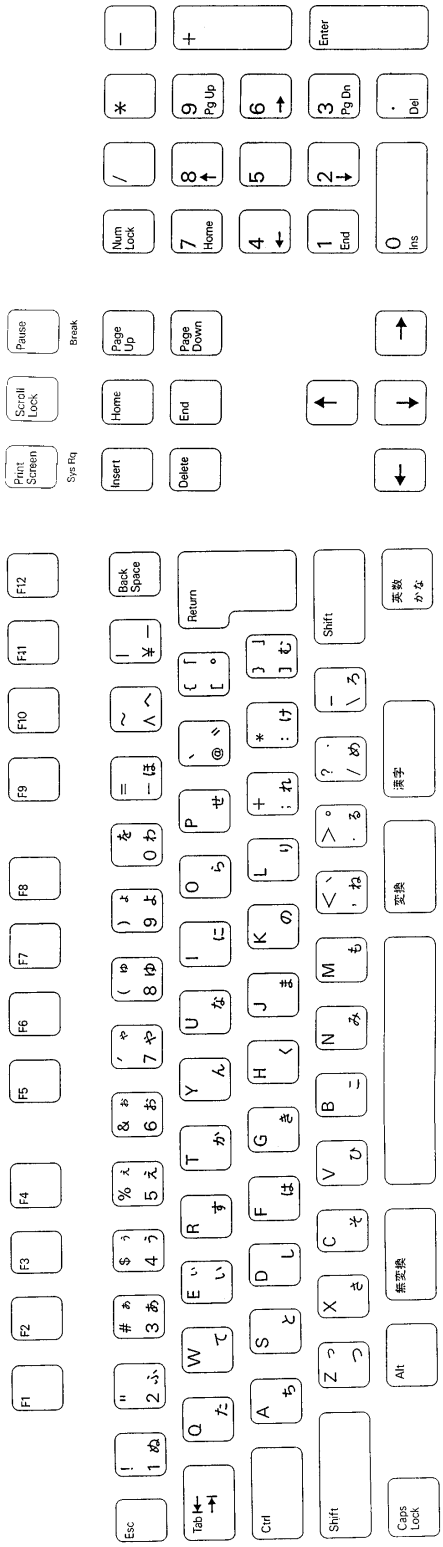

Figure 8–5. Japanese Keyboard

.050
.065
USE ITEMS 41 AND 55
FOR SETUP
3 PRINT LOCATION
3 USE THE "PRINT LOCATION" DIAGRAM FOR ON LINE PAD PRINT SETUP.
2. COPIES OF THE ORIGINAL DRAWING MAY BE USED AS AN INSPECTION
AID FOR THE PURPOSE OF CUSTOMER APPROVAL OF THE LEGEND LAYOUT,
AS WELL AS IDENTIFICATION OF KEYTOP MISLOADS OR MISLOCATED
CHARACTERS ON KEYTOPS. THE TOLERANCES NOTED BELOW ARE APPLIED
TO THE DRAWING ONLY. THESE TOLERANCES DO NOT APPLY WHEN THIS
DRAWING IS USED FOR PURPOSES OTHER THAN THOSE LISTED ABOVE.

Figure 8–6. Korean Keyboard

.065
USE ITEMS 41 AND 55 FOR SETUP
3 PRINT LOCATION
3 USE THE "PRINT LOCATION" DIAGRAM FOR ON LINE PAD PRINT SETUP.
2. COPIES OF THE ORIGINAL DRAWING MAY BE USED AS AN INSPECTION AID FOR THE PURPOSE OF CUSTOMER APPROVAL OF THE LEGEND LAYOUT, AS WELL AS IDENTIFICATION OF KEYTOP MISLOADS OR MISLOCATED CHARACTERS ON KEYTOPS. THE TOLERANCES NOTED BELOW ARE APPLIED TO THE DRAWING ONLY. THESE TOLERANCES DO NOT APPLY WHEN THIS DRAWING IS USED FOR PURPOSES OTHER THAN THOSE LISTED ABOVE.
DRAWING ±.015 - INDIVIDUAL LEGEND LOCATION FROM PN3000 BOM.
TOLERANCES: ±.100 - DISTANCE BETWEEN REGISTRATION KEYTOPS AS NOTED IN THE PRINT LOCATION DIAGRAM (DUE TO DRAWING REPRODUCTION).

Figure 8–7. Norwegian Keyboard

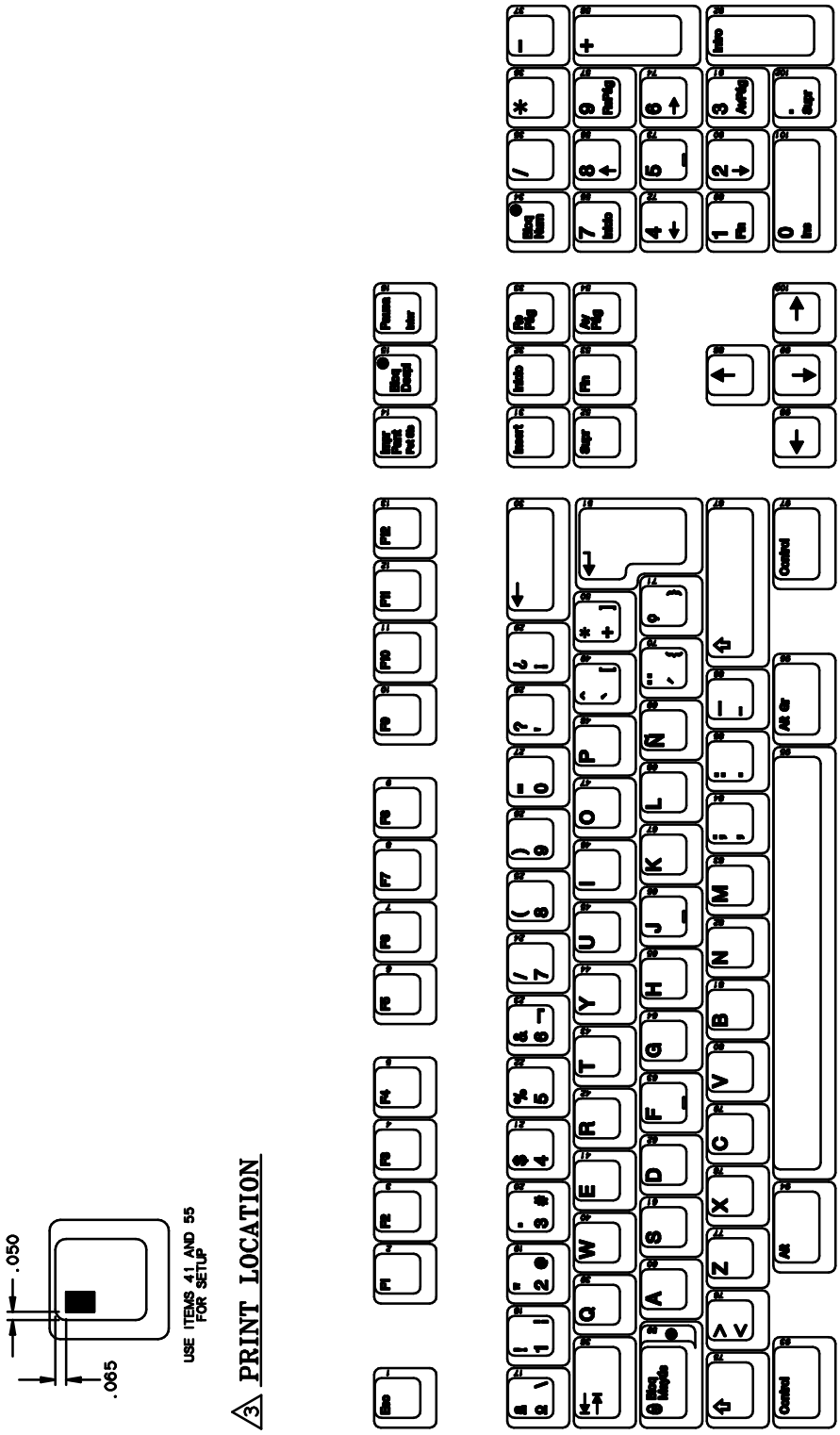

Figure 8–8. Spanish Keyboard

.050
.065
USE ITEMS 41 AND 55 FOR SETUP
3 PRINT LOCATION
3 USE THE "PRINT LOCATION" DIAGRAM FOR ON LINE PAD PRINT SETUP.
2. COPIES OF THE ORIGINAL DRAWING MAY BE USED AS AN INSPECTION AID, FOR THE PURPOSE OF CUSTOMER APPROVAL OF THE LEGEND LAYOUT, AS WELL AS IDENTIFICATION OF KEYTOP MISLOADS OR MISLOCATED CHARACTERS ON KEYTOPS. THE TOLERANCES NOTED BELOW ARE APPLIED TO THE DRAWING ONLY. THESE TOLERANCES DO NOT APPLY WHEN THIS DRAWING IS USED FOR PURPOSES OTHER THAN THOSE LISTED ABOVE.

Figure 8–9. Swedish Keyboard

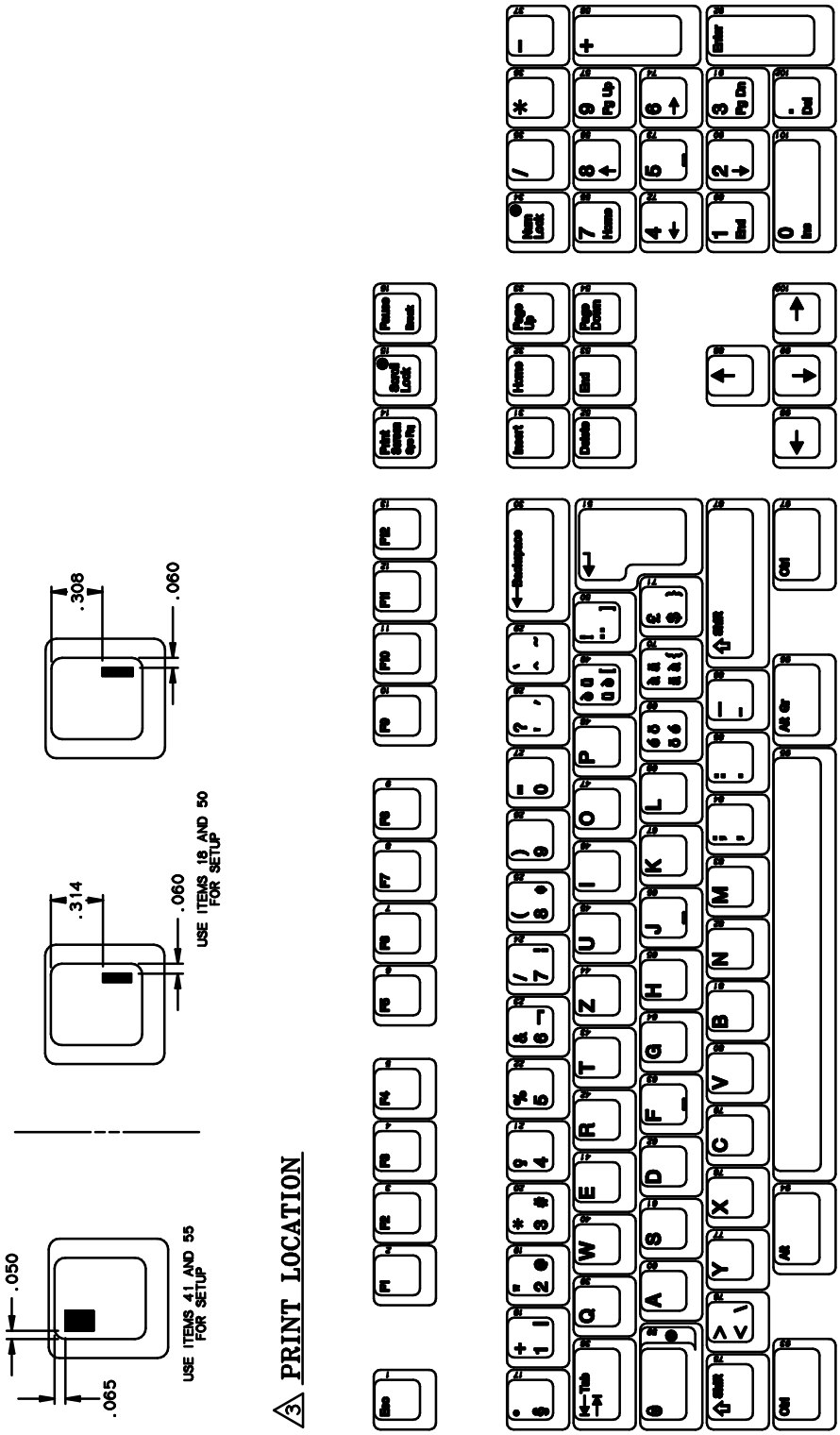

Figure 8–10. Swiss Keyboard

.050
.065
USE ITEMS 41 AND 55
FOR SETUP
3 PRINT LOCATION
3 USE THE "PRINT LOCATION" DIAGRAM FOR ON LINE PAD PRINT SETUP.
2. COPIES OF THE ORIGINAL DRAWING MAY BE USED AS AN INSPECTION
AID, FOR THE PURPOSE OF CUSTOMER APPROVAL OF THE LEGEND LAYOUT,
AS WELL AS IDENTIFICATION OF KEYTOP MISLOADS OR MISLOCATED
CHARACTERS ON KEYTOPS. THE TOLERANCES NOTED BELOW ARE APPLIED

Figure 8–11. Taiwanese Keyboard

.050
.065
USE ITEMS 41 AND 55
FOR SETUP
3 PRINT LOCATION
3 USE THE "PRINT LOCATION" DIAGRAM FOR ON LINE PAD PRINT SETUP.
2. COPIES OF THE ORIGINAL DRAWING MAY BE USED AS AN INSPECTION
AID. FOR THE PURPOSE OF CUSTOMER APPROVAL OF THE LEGEND LAYOUT,
AS WELL AS IDENTIFICATION OF KEYTOP MISLOADS OR MISLOCATED

Figure 8–12. United Kingdom Keyboard

.050
.065
USE ITEMS 41 AND 55 FOR SETUP
3 PRINT LOCATION
3 USE THE "PRINT LOCATION" DIAGRAM FOR ON LINE PAD PRINT SETUP.
2. COPIES OF THE ORIGINAL DRAWING MAY BE USED AS AN INSPECTION AID, FOR THE PURPOSE OF CUSTOMER APPROVAL OF THE LEGEND LAYOUT, AS WELL AS IDENTIFICATION OF KEYTOP MISLOADS OR MISLOCATED CHARACTERS ON KEYTOPS. THE TOLERANCES NOTED BELOW ARE APPLIED TO THE DRAWING ONLY. THESE TOLERANCES DO NOT APPLY WHEN THIS DRAWING IS USED FOR PURPOSES OTHER THAN THOSE LISTED ABOVE.

Figure 8–13. United States Keyboard

For:root
Printed on:Wed, Sep 4, 1996 12:46:15
From book:skyhawk_tech_ref
Document:ch_9
Last saved on:Tue, Mar 12, 1996 09:02:22

9

Connector Pinouts

Slot Connectors

EISA Slots

Table 9−1 lists the EISA Slot connector's pin numbers and signals.

Table 9–1. RS–232 Connectors (2) EISA Slot Connector Pinout

Pin No.	Signal	Pin No.	Signal
Row F		**Row B**	
1	GROUND	1	GROUND
2	+5V	2	RESDRV
3	+5V	3	+5V
4	NC	4	IRQ<9>
5	NC	5	–5V
6	ACCESS KEY	6	DRQ<2>
7	NC	7	–12V
8	NC	8	NOWS*
9	+12V	9	+12V
10	M–10	10	GROUND
11	LOCK*	11	SMWTC*
12	RESERVED	12	SMRDC*
13	GROUND	13	IOWC*
14	RESERVED	14	IORC*
15	BE*<3>	15	DAK*<3>
16	ACCESS KEY	16	DRQ<3>
17	BE*<2>	17	DAK*<1>
18	BE*<0>	18	DRQ<1>
19	GROUND	19	REFRESH*
20	+5V	20	BCLK
21	LA*<29>	21	IRQ<7>
22	GROUND	22	IRQ<6>
23	LA*<26>	23	IRQ<5>
24	LA*<24>	24	IRQ<4>
25	ACCESS KEY	25	IRQ<3>
26	LA<16>	26	DAK*<2>
27	LA<14>	27	T–C
28	+5V	28	BALE
29	+5V	29	+5
30	GROUND	30	OSC
31	LA<10>	31	GROUND

(Continued)

Table 9−1. EISA Slot Connector Pinout (Cont.)

Pin No.	Signal	Pin No.	Signal
Row E		**Row A**	
1	CMD*	1	IOCHK*
2	START*	2	D<7>
3	EXRDY	3	D<6>
4	EX32*	4	D<5>
5	GROUND	5	D<4>
6	ACCESS KEY	6	D<3>
7	EX16*	7	D<2>
8	SLBURST*	8	D<1>
9	MSBURST*	9	D<0>
10	W–R	10	CHRDY
11	GROUND	11	AENx
12	RESERVED	12	SA<19>
13	RESERVED	13	SA<18>
14	RESERVED	14	SA<17>
15	GROUND	15	SA<16>
16	ACCESS KEY	16	SA<15>
17	BE*<1>	17	SA<14>
18	LA*<31>	18	SA<13>
19	GROUND	19	SA<12>
20	LA*<30>	20	SA<11>
21	LA*<28>	21	SA<10>
22	LA*<27>	22	SA<9>
23	LA*<25>	23	SA<8>
24	GROUND	24	SA<7>
25	ACCESS KEY	25	SA<6>
26	LA<15>	26	SA<5>
27	LA<13>	27	SA<4>
28	LA<12>	28	SA<3>
29	LA<11>	29	SA<2>
30	GROUND	30	SA<1>
31	LA<9>	31	SA<0>

(Continued)

Table 9−1. EISA Slot Connector Pinout (Cont.)

Pin No.	Signal	Pin No.	Signal
Row H		**Row D**	
1	LA<8>	1	M16*
2	LA<6>	2	IO16*
3	LA<5>	3	IRQ<10>
4	+5V	4	IRQ<11>
5	LA<2>	5	IRQ<12>
6	ACCESS KEY	6	IRQ<13>
7	D<16>	7	IRQ<14>
8	D<18>	8	DAK*<0>
9	GROUND	9	DRQ<0>
10	D<21>	10	DAK*<5>
11	D<23>	11	DRQ<5>
12	D<24>	12	DAK*<6>
13	GROUND	13	DRQ<6>
14	D<27>	14	DAK*<7>
15	ACCESS KEY	15	DRQ<7>
16	D<29>	16	+5V
17	+5V	17	MASTER16*
18	+5V	18	GROUND
19	MAKx*		
Row G		**Row C**	
1	LA<7>	1	SBHE*
2	GROUND	2	LA<23>
3	LA<4>	3	LA<22>
4	LA<3>	4	LA<21>
5	GROUND	5	LA<20>
6	ACCESS KEY	6	LA<19>
7	D<17>	7	LA<18>
8	D<19>	8	LA<17>
9	D<20>	9	MRDC*
10	D<22>	10	MWTC*
11	GROUND	11	D<8>
12	D<25>	12	D<9>
13	D<26>	13	D<10>
14	D<28>	14	D<11>
15	ACCESS KEY	15	D<12>
16	GROUND	16	D<13>
17	D<30>	17	D<14>
18	D<31>	18	D<15>
19	MREQ*		

* Active Low

F/W Differential SCSI Connector

The F/W SCSI connector is part number 1252–4426, a 68–pin high–density D–sub right–angle connector.

Table 9–2. RS–232 Connectors (2) Fast, Wide Differential SCSI Connector Pinout

Pin	Signal Name	Pin	Signal Name
1	FW_SD12+	35	FW_SD12–
2	FW_SD13+	36	FW_SD13–
3	FW_SD14+	37	FW_SD14–
4	FW_SD15+	38	FW_SD15–
5	FW_SP1+	39	FW_SP1–
6	Gnd	40	Gnd
7	FW_SD0+	41	FW_SD0–
8	FW_SD1+	42	FW_SD1–
9	FW_SD2+	43	FW_SD2–
10	FW_SD3+	44	FW_SD3–
11	FW_SD4+	45	FW_SD4–
12	FW_SD5+	46	FW_SD5–
13	FW_SD6+	47	FW_SD6–
14	FW_SD7+	48	FW_SD7–
15	FW_SP0+	49	FW_SP0–
16	FW_DIFFSENS	50	Gnd
17	FW_TERM POWER	51	FW_TERM POWER
18	FW_TERM POWER	52	FW_TERM POWER
19	not connected	53	not connected
20	FW_SATN+	54	FW_SATN–
21	Gnd	55	Gnd
22	FW_SBSY+	56	FW_SBSY–
23	FW_SACK+	57	FW_SACK–
24	FW_SRST+	58	FW_SRST–
25	FW_SMSG+	59	FW_SMSG–
26	FW_SSEL+	60	FW_SSEL–
27	FW_SCD+	61	FW_SCD–
28	FW_SREQ+	62	FW_SREQ–
29	FW_SIO+	63	FW_SIO–
30	Gnd	64	Gnd
31	FW_SD8+	65	FW_SD8–
32	FW_SD9+	66	FW_SD9–
33	FW_SD10+	67	FW_SD10–
34	FW_SD11+	68	FW_SD11–